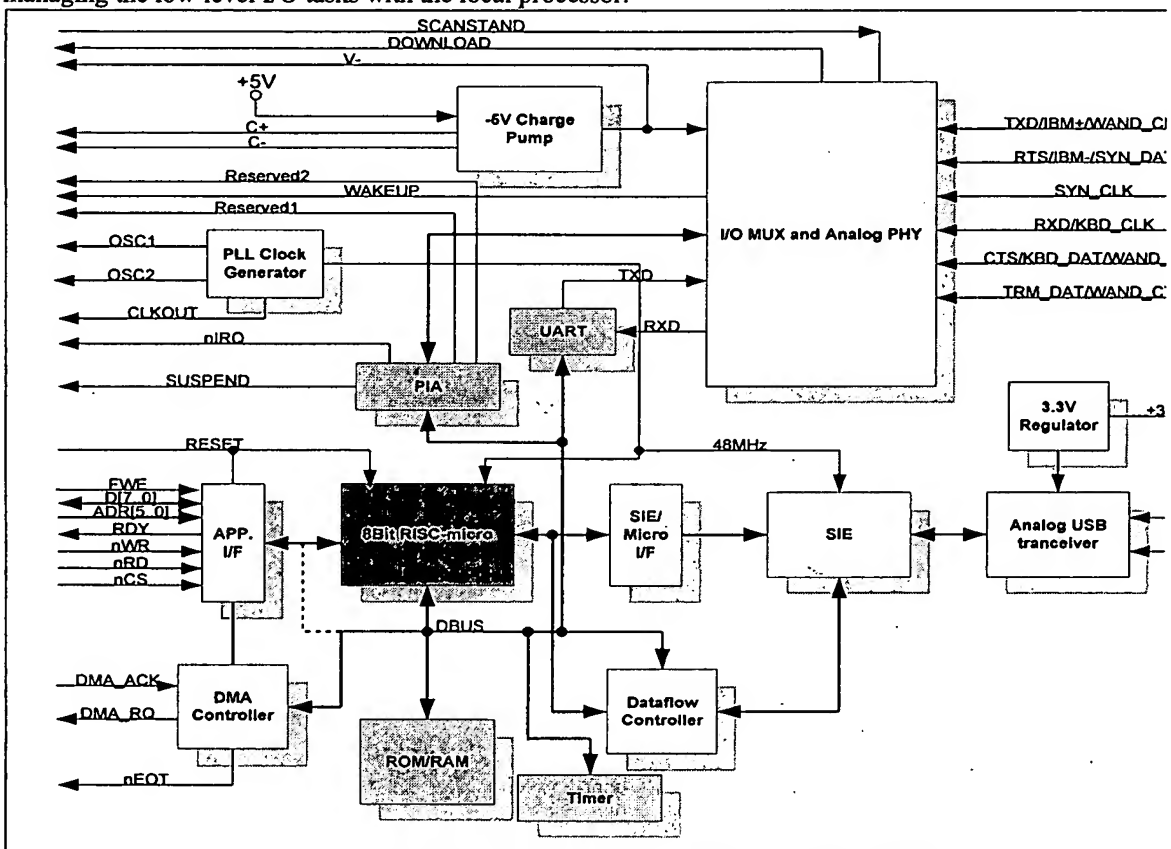
EXHIBIT C

A new Multi-interface Controller ASIC approach

Background

As primitive as the proposed Multi-Interface ASIC is, the integration of this multi-interface ASIC will require enormous processing power from the local processor. Moreover, it will likely be demanding a higher performance processor than what it would otherwise suit for the application. Hence, the product cost will rise and this will especially effect the low-end products. The other drawback will be the reduction of software reusability while integrating this ASIC design across various platforms comparing to the more modular Synapse lump implementation.

One approach toward solving these problems is to make a multi-interface controller that handles link level control for all enclosed interfaces. This local processor will then control these interfaces through the device via its application interface. A universal I/O control will be provided for all I/O interfaces so that it will be as friendly as if it is using an UART or a HDLC controller. This will certainly alleviate the burden of managing the low-level I/O tasks with the local processor.



block diagram for multi-interface controller ASIC

How will this work?

In this new approach, an embedded processor will emulate the USB endpoints. As what is illustrated in the above diagram, the SIE is responsible for bit stuffing/unstuffing, CRC and DPLL and the embedded processor handles the USB data flows, house-keeping as well as communicating with outside host processor. By further extending the processor with a UART, a PIA and a Timer, it will be fully equipped to emulate various interface protocols. The block labeled the 'I/O Mux and Analog PHY' is the same block as what was on the original ASIC specification, whose function is to multiplex I/O pins among multiple interface types. The convention used on the diagram is that all signals on the left side of the diagram get

connected to a local processor while signals on the right side get connected to the modular jack. As such, this embedded processor can be used to emulate and to route I/O through different interfaces, such as RS-232, IBM 468x, Synapse, Keyboard Wedge, Wand Emulation, and USB. Likewise, it can also be used to handle various I/O modes. Similar to a bus friendly peripheral device, this ASIC will do character based I/O, packet, DMA transfer as well as event interrupts to the local CPU. Controls and data to and from this ASIC will be transferred via its mailbox interface. It is noted here that the **USB burst and Isochrous mode will only be implemented with DMA.**

When the embedded processor detects the absence of SOF packet, it will subsequently assert the SUSPEND signal, then switch itself to low-power mode.

Programming Interface

The programming and control of each I/O is done via the bi-directional mailbox interface. Their enclosed input/output registers are mapped per interface selection. For instance, whenever the character based I/O, these registers will be input, output and status registers similar to what is on a standard UART. Likewise, in packet based I/O, these registers will then be used to setup DMA transfer and a respective register will be used to reflect the status of I/O buffers status. An interrupt is used to notify local processor upon events on selected interface such as data arrival or end of transmission or other I/O conditions. The DMA channel is provided to reduce overhead incurs during data transfer between the controller and local processor. This is especially in the high-speed packet transfer such as USB.

Benefit of this design

By implementing the USB control with a general-purpose processor gives rise to the capability of managing other I/O protocols without adding complexity to the ASIC. The resulting universal I/O interface simplifies the I/O software resides in the local process. Besides, the embedded flash ROM will allow future update. This can potentially prevent any costly wafer re-spin. The USB power management, especially during power up enumeration and suspend, will also be conveniently handled by this embedded processor.

What will the obstacles be?

There is obstacle lay ahead of us. Although the implementation of the added processor, UART and PIA seems to add more gates to the original design, the required ROM (16K or more) posts an even great challenge to those suppliers whom we have successfully solicited. Since most of them does not have the capability to embed FLASH in their wafer process. In addition, there will be unit cost and NRE cost impact in this design approach. Since there will be modifications that need to be made from the off-the-shelf USB core, the risk level will be higher than the other alternative despite all the benefits mentioned earlier. This means prototyping will be desirable to ensure its performance prior to committing it to silicon. A full-time hardware/software development support will be sustained for months.

EXHIBIT D

Schedule Estimate for PSC Standard Range Replacement Product Utilizing a Fuzzy MercImp based "Decoded" Engine

Overview: This product would utilize a Fuzzy MercImp based decoded engine in conjunction with a Toshiba based decoder. The "decoded" engine would do the front end processing of the barcode data, converting the strength and timing signals into DBP that would passed to the Toshiba decoder. The decoder would then decode the DBP and transmit the data via MIA. This decoder architecture would be same as that used in both NG Smartline and NG Hot Shot 1D with the addition of external I/O multiplexing allow the product to meet PSC pin out requirements.

Assumptions:

1 The MercImp based Fuzzy Engine would use existing Opto/ Mechanical/ Focusing components.
2 DBP "conversion" S/W would be available in four weeks from start of project.
3 AD associate available for consultation as required – expected to minimal unless chip issues arise.
4 Can resolve Power on/down issues to make engine look like existing dumb engines.
5 Project is given very high priority (PCB Resources, Technicians etc. are available)

Schedule Estimates: (2 fully loaded Analog Engineers, 1 fully loaded Digital Engineer). Duration indicates best case elapsed time. Initial plan had 1 fully loaded Analog and 1 fully loaded Digital Engineer)

Engine Development	Duration (Weeks)	Handleboard Development	Duration(Weeks)
System Design Issues (Powerdown, interface, etc.)	1	I/O Muxing for PSC pin outs	1
1st Cut Schematic	1	Schematic for Dev. PCB	1
PCB Layout/ Review	1	PCB Layout/ Review	1
Procure/build proto (BGA MercImp available)	1	Procure/ build Proto	1
Test / Optimize H/W (develop E2 params, analog chain verified)	2	Test/ debug proto	1
2nd Spin PCB		Form factor PCB	
Schematic/PCB mods	1	Schematic/PCB mods	2
Procure/build protos	1	Procure/build protos (need QFP MIA)	1
Test/debug protos	1	Test/debug protos	1
Total Development time/ (effort)	9 weeks / (18 manweeks)	Total Development effort	9 weeks
Engineering Verification Testing (need product S/W to verify functionality)			4
Pilot Build (			???
Qual Test (Could run in parallel with Eng. Verification to reduce overall calendar time)			6

know what we don't know.

2 System design issues – system performance/ aggressiveness is unknown due to power up issues and time lag to decode. Can engine be designed to "just drop in" to existing decoders both for scanners and terminals

3 This will impact the Lorax version development – shared resources (I suspect that Optics will be the resource constraint in that effort)

4 System will cost more than using an undecoded Engine (Flash cost, crystal, supervisory ckt, miniaturization premiums, etc.)

5 Integration of MercImp goes smoothly – works as expected. History tells us this is a significant risk.

Conclusion:

If we are serious about trying to accelerate this program, using a MercImp based Fuzzy engine in conjunction with a Toshiba based decoder seems to be the only shot of pulling in the date. If we are all willing to accept the risk that is inherint in this approach (first product to incorporate MercImp) and assign it the necessary priority it needs, then we should quickly decide to follow this course and execute the program as efficiently as possible.

EXHIBIT E

MULTI-INTERFACE ASIC

SPECIFICATION

PRELIMINARY

Symbol Technologies Inc.
One Symbol Plaza
Holtsville, New York 11742-1300

Revision: 6 Date: 3/26/2001

Confidential

Revision History

Revisoin	Issue Date	Comment
1		First draft 5/1/2000 TC
2		Added LED drivers and updated bus specifications 5/11/2000
3		Changed the USB controller to a generic controller with SIE and UART timer plus OCIA interface
4		Changed the controller to a 8051 core Modified the mailbox to 8 slots 1/14/01 Revised the I/O control and the USB tranceiver spec. 1/23/01
5		Corrected few errors in the spec. 2/12/01 Modified the wake up detection section to eliminate the 32KHz clock in suspend mode. Added pull-up resistor on RESET and CS, and pull-down resistor on FWE. Added the PSEN signal on the ICE version. Changed the cap. To 0.22uF on charge-pump. Added the low-power control on RS-232 output.
6		Changes made on the Digital I/O to be 3.3V and 5V tolerant. A I/O pin was spared to be the VCCIO to bring I/O voltage to the chip.

Conventions

1. All voltage specifications for input/output pins are referred to GND, unless otherwise specified.

Reference Documents:

1. The *IBM-AT Hardware Technical Reference Manual*
2. Maxim MAX1485 Data Sheet.
3. Analog Devices ADM101E Data Sheet.
4. Micrel MIC2550 Data Sheet.
5. Philips PDIUSBD12 Data Sheet.
6. Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (ANSI/TIA/EIA-232-F-1997)
7. USB 1.1 Specification
8. Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems (ANSI/TIA/EIA-485-A-98)
9. NCR 250-0006186 OCIA Interface Document

2. Glossary and Definitions

RS-232: The EIA standard was adopted in 1975 for serial data communication. It is a common communication interface standard that permits DTEs and DCEs to connect successfully.

RS-485: It is similar to RS-232 except it uses a balanced (differential) media and carries signal in both directions.

Charge Pump: A way to convert/invert DC voltage by using switches or diodes.

Synapse: This is a bi-directional serial interface.

Wand Emulation: As it seems, it is to emulate the old Wand bar-code reader. It consists of a clock signal along with digital bar-code pattern. This is a unidirectional serial interface.

Keyboard Wedge: The keyboard plugs into the wedge and the wedge device plugs into the computer where the keyboard was.

USB: Universal Serial Bus is a serial communication standard.

OCIA: Optically Coupled Interface Adapter is a bi-directional serial interface. It uses clocks to synchronize data during communication. The clock is always originated from the receiving (Host) end.

UART: Universal Asynchronous Receiver Transmitter.

PPIA: Programmable Parallel Interface Adapter.

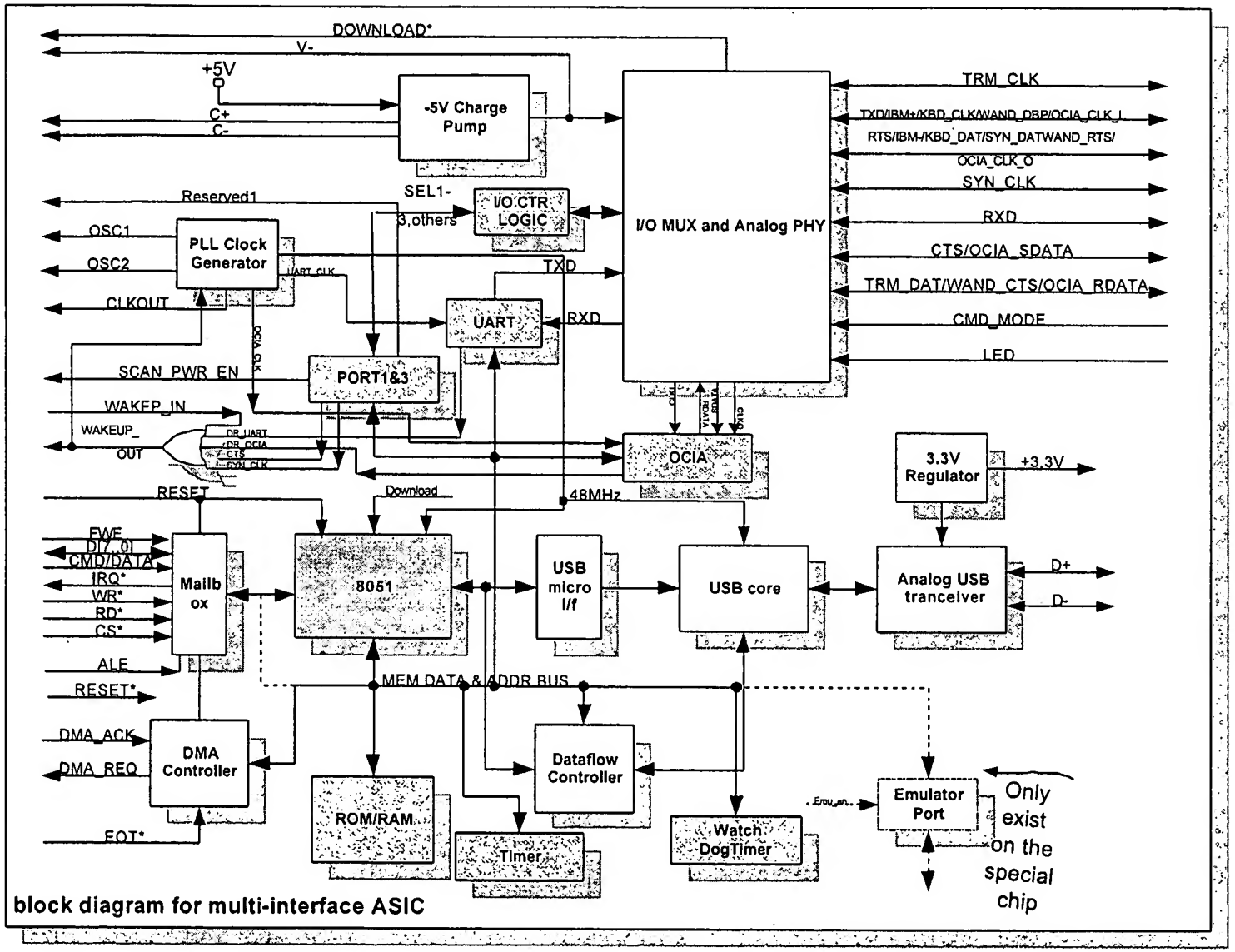
Application

The chip is going to be used in a POS device to provide greatest adaptability toward different I/O functions. In addition, it fits all I/O configurations in a 10-pin connector. There are two versions of chips specified herein. One is the normal chip without additional test pads and the other is the special package chip with extra pins for using with an 8051 In-Circuit-Emulator.

Block Diagram

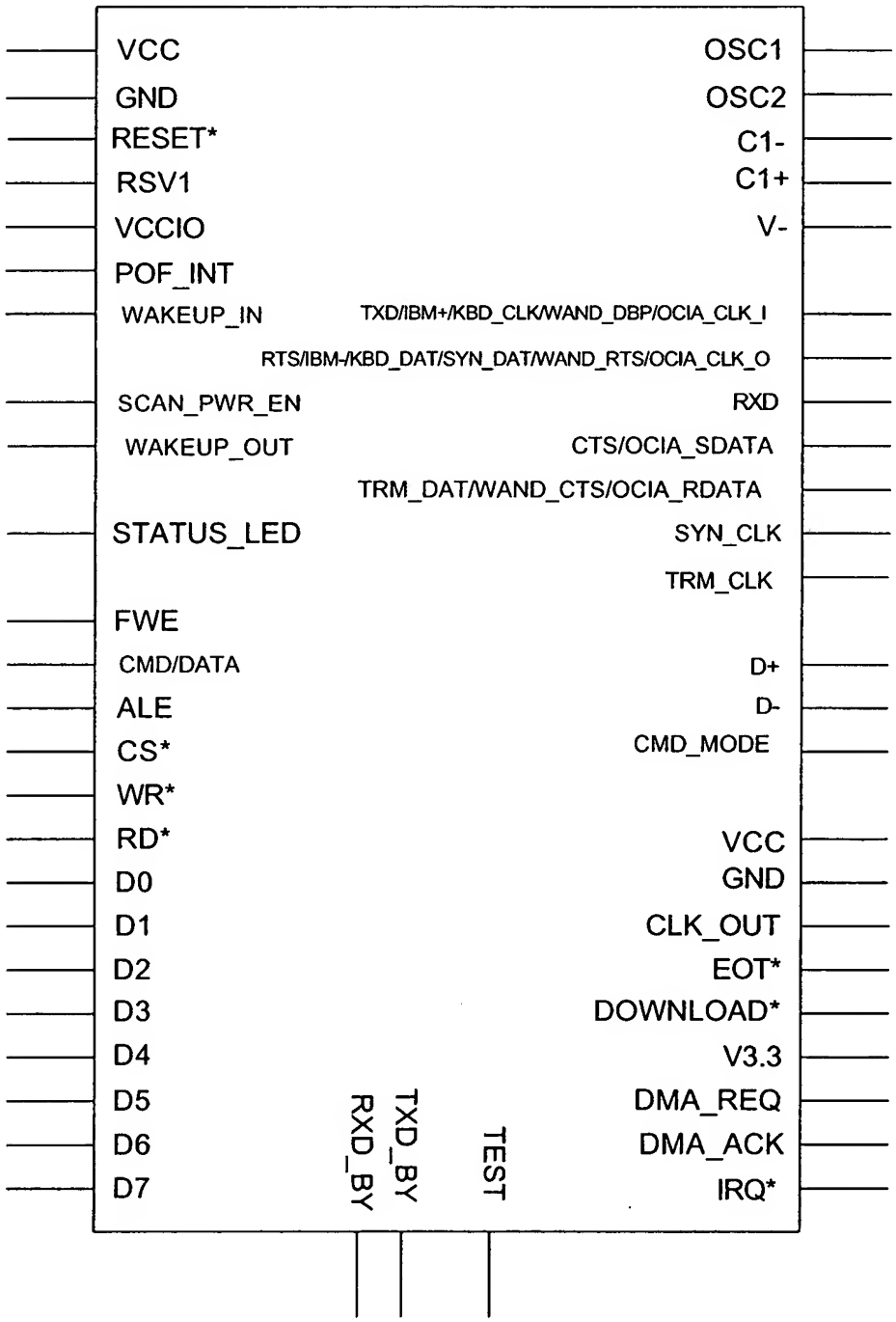
The detail block diagram of this multi-interface controller ASIC is depicted in the following diagram. It accommodates seven different I/O functions. The internal 8051 processor can select any one of these seven interfaces. Eight out of ten connector pins are shared among these interfaces. The required I/O signals for each function are:

USB:	D+, D- inout;
RS-232:	TXD, RTS out; RXD,CTS in;
RS-485:	IBM+, IBM- inout;
KBD Wedge:	KBD_CLK, KBD_DAT inout; TRM_CLK, TRM_DAT inout;
Synapse:	SYN_CLK, SYN_DAT inout;
Wand Emul:	WAND_RTS, WAND_DBP out; WAND_CTS in;
OCIA	OCIA_SDATA,OCIA_CLKIN, OCIA_CLKOUT in; OCIA_RDATA out;



block diagram for multi-interface ASIC

Figure 2. The chip outline

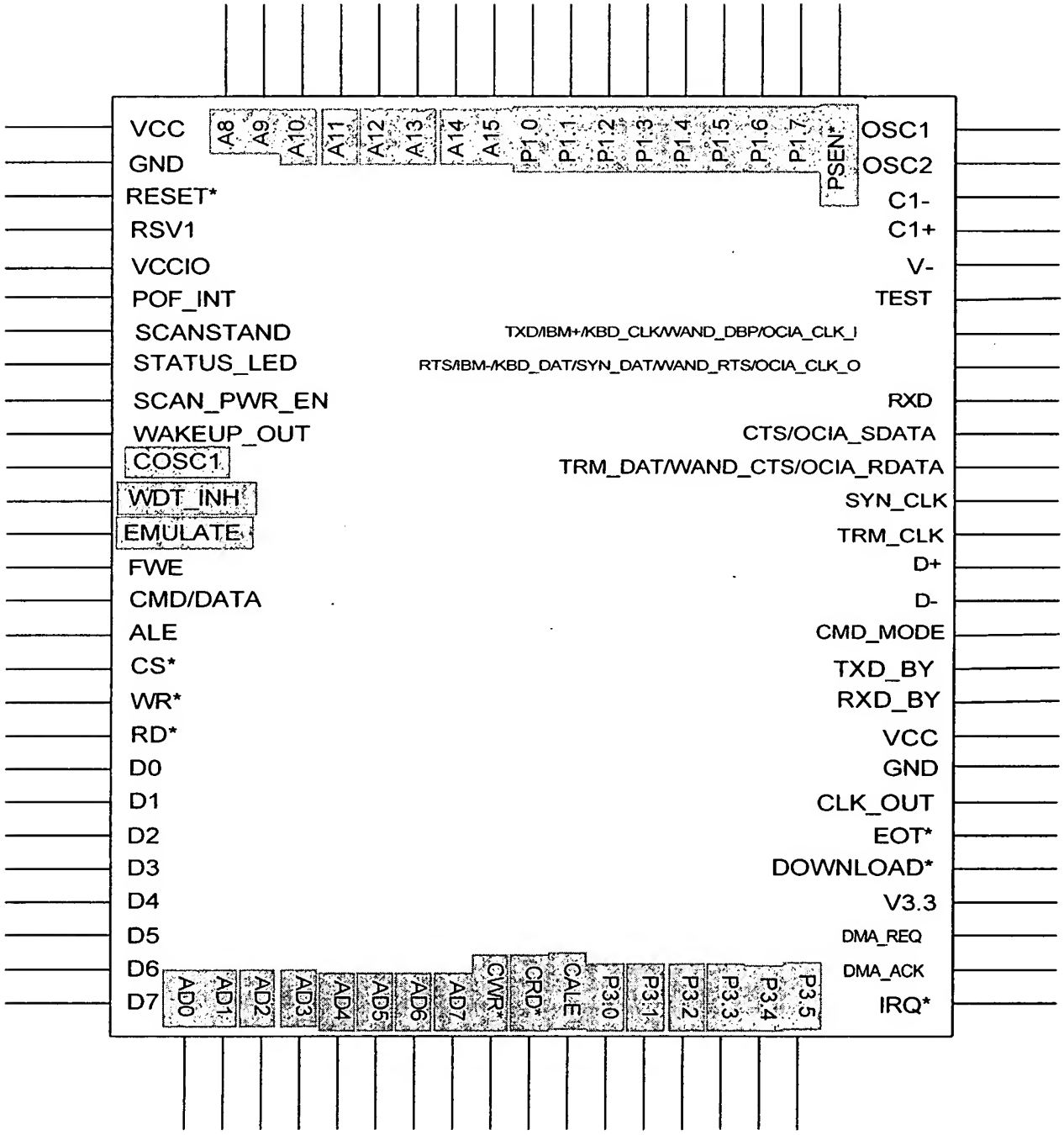


The I/O pin definition

VCC	Power		2	Nominal +5V
GND	Power		2	Ground
C1+			1	positive side of voltage inversion capacitor
C1-			1	negative side of voltage inversion capacitor
V-			1	-5V output out of charge pump
V3.3	Power	Out	1	Regulated 3.3V out
WAKEUP_OUT	Digital	Out	1	
TEST	Digital	In	1	Dedicated test pin
Spares	Digital	Out	1	Spare PPIA output for future use
VCCIO	Power	In	1	Digital I/O cell power supply
POF_INT	Digital	Out	1	POF interrupt
ALE	Digital	In	1	Address latch enable, used on multiplex address/data mode
WAKEUP_IN	Digital	In	1	External Wakeup input (for wakeup)
OSC1-2	Passive		2	Crystal inputs or Resonator inputs
D0-7	Digital	In/Out	8	8 bit data bus
RD*	Digital	In	1	Read Strobe
WR*	Digital	In	1	Write Strobe
FWE	Digital	In	1	Flash Write Enable
CMD/DATA	Digital	In	1	address/Data indicator used on non-multiplex mode
CS*	Digital	In	1	Chip Select
SCAN_PWR_EN	Digital	Out	1	Scanner Power Enable control
RESET*	Digital	In	1	Master Reset
EOT*	Digital	Out	1	End of DMA transfer
D+	Analog	In/Out	1	USB Differential Positive out
D-	Analog	In/Out	1	USB Differential negative out
TXD/IBM+/KBD_CLK/WAND_DBP/OCIA_CLK_I	Analog	In/Out	1	RS-232 TXD/485 Differential Pos/Keyboard clock/Wand DBP/OCIA clock in
RTS/IBM-/SYN_DAT/KBD_DAT/WAND_RTS/OCIA_CLK_O	Analog	In/Out	1	RS-232 RTS/485 Differential Neg/Synapse DATA/Keyboard DATA/Wand RTS/OCIA clk out
DOWNLOAD*	Digital	Out	1	Download flag
RXD	Analog	In	1	RS-232 RXD signal
CTS/OCIA_SDATA	Analog	In	1	RS-232 CTS/Keyboard data
TRM_CLK	Analog	In/Out	1	Terminal Clock
TRM_DAT/WAND_CTS/OCIA_RDATA	Analog	In/Out	1	Terminal DATA/Wand CTS/OCIA RDATA
SYNC_CLK	Analog	In/Out	1	Synapse Clock
CLK_OUT	Digital	Out	1	Programmable Clock generator
DMA_REQ*	Digital	Out	1	DMA request
DMA_ACK	Digital	In	1	DMA acknowledged
IRQ*	Digital	Out	1	Interrupt Request
CMD_MODE	Digital	In	1	Command mode flag
STATUS_LED	Analog	Out	1	Status LED drive
TXD_BY	Digital	Out	1	RS-232 TXD Bypass
RXD_BY	Digital	In	1	RS-232 RXD Bypass

Total Pin	51

The chip outline of special bond out chip



The I/O pin definition for the special chip

Pin Name	Dig/Ana	In/Out	no. Pin	Description
VCC	Power		2	Nominal +5V
GND	Power		2	Ground
C1+			1	Positive side of voltage inversion capacitor
C1-			1	Negative side of voltage inversion capacitor
V-			1	-5V output out of charge pump
V3.3	Power	Out	1	Regulated 3.3V out
WAKEUP_OUT	Digital	Out	1	
TEST	Digital	In	1	Dedicated test pin
Spares	Digital	Out	1	Spare PPIA output for future use
VCCIO	Power	In	1	Digital I/O voltage
POF_INT	Digital	Out	1	USB Pulse of Frame signal
ALE	Digital	In	1	Address Latch Enable used on multiplex address/data mode
WAKEUP_IN	Digital	In	1	External wakeup input
OSC1-2	Passive		2	Crystal inputs or Resonator inputs
D0-7	Digital	In/Out	8	8 bit data bus
RD*	Digital	In	1	Read Strobe
WR*	Digital	In	1	Write Strobe
FWE	Digital	In	1	Flash Write Enable
CMD/DATA	Digital	In	1	CMD(address) or DATA
CS*	Digital	In	1	Chip Select
SCAN_PWR_EN	Digital	Out	1	Scanner power enable
RESET*	Digital	In	1	Master Reset
EOT*	Digital	Out	1	End of DMA transfer
D+	Analog	In/Out	1	USB Differential Positive out
D-	Analog	In/Out	1	USB Differential negative out
TXD/IBM+/KBD_CLK/WAND_DBP/OCIA_CLK_I	Analog	In/Out	1	RS-232 TXD/485 Differential Pos/Keyboard clock/Wand DBP/OCIA clock in
RTS/IBM-/SYN_DAT/KBD_DAT/WAND_RTS/OCIA_CLK_O	Analog	In/Out	1	RS-232 RTS/485 Differential Neg/Synapse DATA/Keyboard DATA/Wand RTS/OCIA clk out
DOWNLOAD*	Digital	Out	1	Download flag
RXD	Analog	In	1	RS-232 RXD
CTS/OCIA_SDATA	Analog	In	1	RS-232 CTS/Keyboard data
TRM_CLK	Analog	In/Out	1	Terminal Clock
TRM_DAT/WAND_CTS/OCIA_RDATA	Analog	In/Out	1	Terminal DATA/Wand CTS/OCIA RDATA
SYNC_CLK	Analog	In/Out	1	Synapse Clock
CLK_OUT	Digital	Out	1	Programmable Clock generator
DMA_REQ*	Digital	Out	1	DMA request
DMA_ACK	Digital	In	1	DMA acknowledged
IRQ*	Digital	Out	1	Interrupt Request
CMD_MODE	Digital	In	1	Command mode flag
STATUS_LED	Analog	Out	1	LED drive transistor
TXD_BY	Digital	Out	1	RS-232 TXD Bypass

RXD_BY	Digital	In	1	RS-232 RXD Bypass
AD7-0	Digital	In/Out	8	8051 Address/Data bus
A15-8	Digital	In/Out	8	8051 Address bus
CWR*	Digital	In/Out	1	8051 Write Strobe
CRD*	Digital	In/Out	1	8051 Read Strobe
CALE	Digital	In/Out	1	8051 Address Latch Enable
P3.0-5	Digital	In/Out	6	8051 Port 3
P1.0-7	Digital	In/Out	8	8051 Port 1
PSEN*	Digital	In	1	8051 PSEN
COSC1	Digital	Out	1	8051 OSC1
EMULATE	Digital	In	1	8051 Emulate enable
WDT_INH	Digital	In	1	WDT Inhibit control

Total Pin 88

The DC Specification

Electrical Specifications

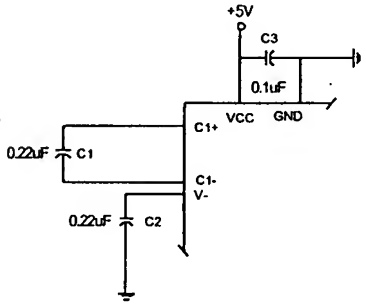
Parameter	Min	Max	Unit	Condition
Supply Current (Normal Mode)		TBD	mA	VCC = 5.25V
Supply Current (Power down Mode)		1 max	mA	VCC = 5.25V with –5V charge pump on
Supply Current (Suspend Mode)		500 max	uA	VCC = 5.25V with –5V charge pump off
Supply Voltage		4.75 - 5.25	V	
Maximum Input Voltage Range	-5	5.7	V	For bipolar I/O pins
	-0.7	5.7	V	For uni-polar I/O pins
Internal Resistors		+/-30	%	At full temperature range

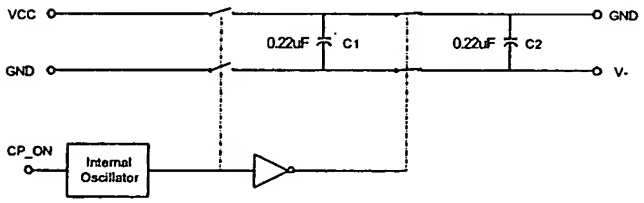
PLL Clock Generator

The PLL is used to multiply (X4) the input crystal or resonant frequency (12MHz) to the required 48MHz clock for the USB core. The clock oscillator shall be made so that either a low-cost crystal or a resonator can be used in application. The start time for the PLL shall be less than 10 ms as specified in the USB specification. There shall be several clock outputs from this block, which are 48MHz, 24MHz, 1.84615MHz (24MHz divided by 13), 300KHz and clock output for external application. The PLL on/off control shall be provided so that the PLL can be turned off via the embedded micro. This PLL_ON_OFF signal is an active low signal, which will keep the PLL oscillator on while it is low. The DPLL of USB SIE uses the 48MHz clock, whereas the CPU uses the 24MHz and 300KHz is used by the WDT.

Charge Pump

The charge pump is used to convert +5V to –5V for the RS-232 transceiver. It is desirable that the charge pump can be shut-off during USB suspend mode. This charge pump will run on a separate oscillator other than the PLL described above. An on/off control is required to turn this charge pump off during the USB suspend. The CP_ON control is an active high signal, which will be turning the charge pump on after power on reset. This CP_ON will be controlled via the internal 8051 processor. It is required to keep this charge pump on during USB mode due to the internal circuit switching speed requirement.





CP_ON: Charge pump on when it is '1'
Charge pump off when it is '0'

Electrical Specifications

Parameter	Typical	Unit	Condition
Internal Oscillator	120K	Hz	
V- Voltage	4.2	V	Total current = 5mA, VCC=5.0V

USB SIE

The USB specification shall comply fully with the USB Specification Rev. 1.1. It will only be configured as a full-speed (12Mbps) peripheral function.

SIE (Series Interface Engine)

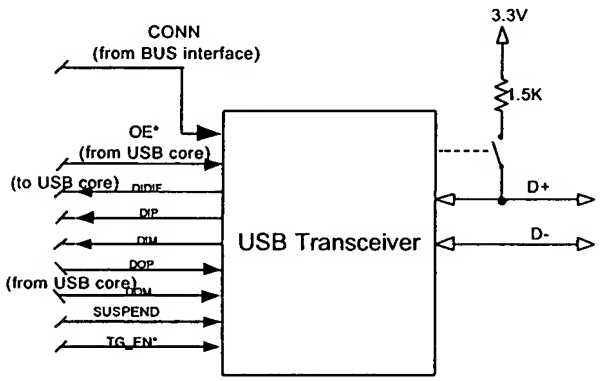
- Serial data transmit and receive
- DPLL receiver clock recovery
- CRC generation/checking
- NRZI encoding/decoding
- Bit stuffing/unstuffing
- Packet Identifier decode
- EOP detection
- Device Reset detection
- Suspend detection
- Stalled detection
- Error Checking
    - CRC error
    - Bit Stuff Errors
    - Sync Field Errors
    - EOP Errors
    - Token Errors
    - Data / Token PID Errors
    - Data Toggle Errors
    - Hand Shake Errors
    - Byte Boundary Errors
    - Error and Transaction Logging
- Support Isochronous mode
    - Provide at least 1 K bytes of end point FIFO memory

Processor

An 8051 or compatible processor running at 4 clocks per machine cycle or faster shall be used. The scratch pad RAM shall be 256 bytes and the total address range shall be no less than 64K bytes. There are at least two UARTs and two timers incorporated, which includes the one used for baud rate generation. There shall be two dedicated ports (e.g. port 1 and 3) available. The CPU will be operated with a 24MHz clock.

USB Transceiver

The USB transceiver is the physical layer of USB. Only the full-speed mode is required in this transceiver design. Thus a 1.5K resistor is connected between 3.3V supply and D+ via a switch to allow connect/disconnect via the control of the 8051 processor. There are total of seven signals connected to/from the USB core. The DIDIF is the single ended differential output and the DIP, DIM, DOP, DOM is differential input and output signals from the USB SIE. The CONN signal is used to engage the pull-up



resistor whenever the USB connection is required. And the TG_EN* (*active low*) signal is used to turn on the internal Transmission Gate to allow the USB output once the USB connection is established. And the USB core will only establish its connection with remote host if and only if valid SETUP packet is received. The CONN signal is controlled through the 8051, where as the TG_EN* is generated by the digital hardware. It is noted that the enabling of pull-up resistors on TRM_CLK and TRM_DAT will automatically negate the TG_EN* in regardless whether the USB connection is still active. The I/O truth table and its electrical specifications are as the following.

SUSPEND	CONN (Note 1)	OE*	DIDIF	DOP	DOM	DIP	DIM	D+	D-	
0	1	1	X	X	X	0	0	D+,(D-)<0.3V, Pull-up Resistor is enabled		Receive
0	1	1	0	X	X	0	1	D->(D+)+0.2V, Pull-up Resistor is enabled		
0	1	1	1	X	X	1	0	D+>(D-)+0.2V, Pull-up Resistor is enabled		
0	1	1	X	X	X	1	1	D-,(D+)>2.7V, Pull-up Resistor is enabled		
0	1	0	X	0	0	0	0	0	0	Transmit
0	1	0	0	0	1	0	1	0	1	
0	1	0	1	1	0	1	0	1	0	
0	1	0	X	1	1	1	1	1	1	
1	1	1 (Note 2)	1	X	X	1	0	Pull-up Resistor is Enabled; D+,D- in Input Mode		Suspend
X	0	1 (Note 2)	X	X	X	X	X	Pull-up Resistor is Opened; D+,D- in Hi-Z mode (same as Input Mode)		Transceiver is Disabled

Note 1 – The CONN going low will mean the USB D+ and D- signals will not be used, such as in the non-USB I/O modes. The CONN signal will control when the D+ and D- drivers are turned off. Whenever the CONN signal is low, the D+ and D- pins will be in high impedance state and the Differential Receiver will be turned off (zero current state).

Note 2 – In either the Suspend Mode or non-USB mode the Transceiver shall automatically be switched to the Input Mode.

Electrical Specifications

Parameter	Typical	Unit	Condition
Logic Input Threshold Low	0.8 max	V	
Logic Input Threshold High	2.4 min	V	
Logic Output High	4.6 min	V	VCC = 5V
Logic Output Low	0.4 max	V	I = 1mA
Transceiver Output Hi Voltage	2.8 - 3.6	V	Rload = 15K
Transceiver Output Lo Voltage	0.3 max	V	Rload = 15K
Transceiver Capacitance	20	PF	Pin to GND
Transceiver Diff. Common Mode	0.8 - 2.5	V	
Transceiver Diff. Input Sensitivity	0.2	V	
Transceiver Input Hysteresis	200	mV	
Transceiver Output Risetime	4-20	ns	Cload = 50pf
Transceiver Output Falltime	4-20	ns	Cload = 50pf
Risetime/Falltime Matching	+/-10%		

Transceiver Output Crossover	1.3 - 2.0	V
The Pull-up resistor	1.1K-1.9K	Ohm
Analog-switch Rds ON	75 max	Ohm
Analog-switch turn-on time	200 max	ns
Analog-switch turn-off time	200 max	ns
Switch feed-thru capacitance	0.5max	PF
Transceiver Input Voltage	±5	V

Bus Interface

The parallel bus interface is used to communicate with the embedded micro as well as with the clock output control. The parallel bus input/output is similar to what is illustrated in the Philips Semiconductor PDIUSBD12 datasheet.

The following specification applies to all Bus Interface logic signals, which include D0-7, WR*, RD*, CS*, ALE, A0, IRQ*, DMA_REQ, DMA_ACK, CLKOUT, EOT*.

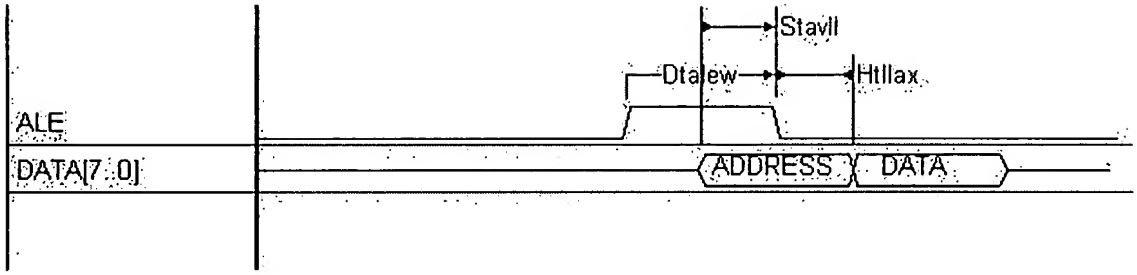
Signal Name	I/O type	Description	Polarity
D0-7	IO	Bi-direction data bus	
CS*	I	Chip select	Negative
ALE	I	Address Latch Enable	
WR*	I	write strobe	Negative
RD*	I	read strobe	Negative
A0	I	Address 1=command, 0=data	
DMA_REQ	O	DMA request	
DMA_ACK	I	DMA acknowledge	
EOT*	I	End Of Transfer	Negative
FWE	I	Flash Write Enable	
IRQ*	O	Interrupt Request	Negative

The Bus Interface I/O will be either 3.3V or 5V depends on the supply voltage applied to the VCCIO and its electrical specification is as the following:

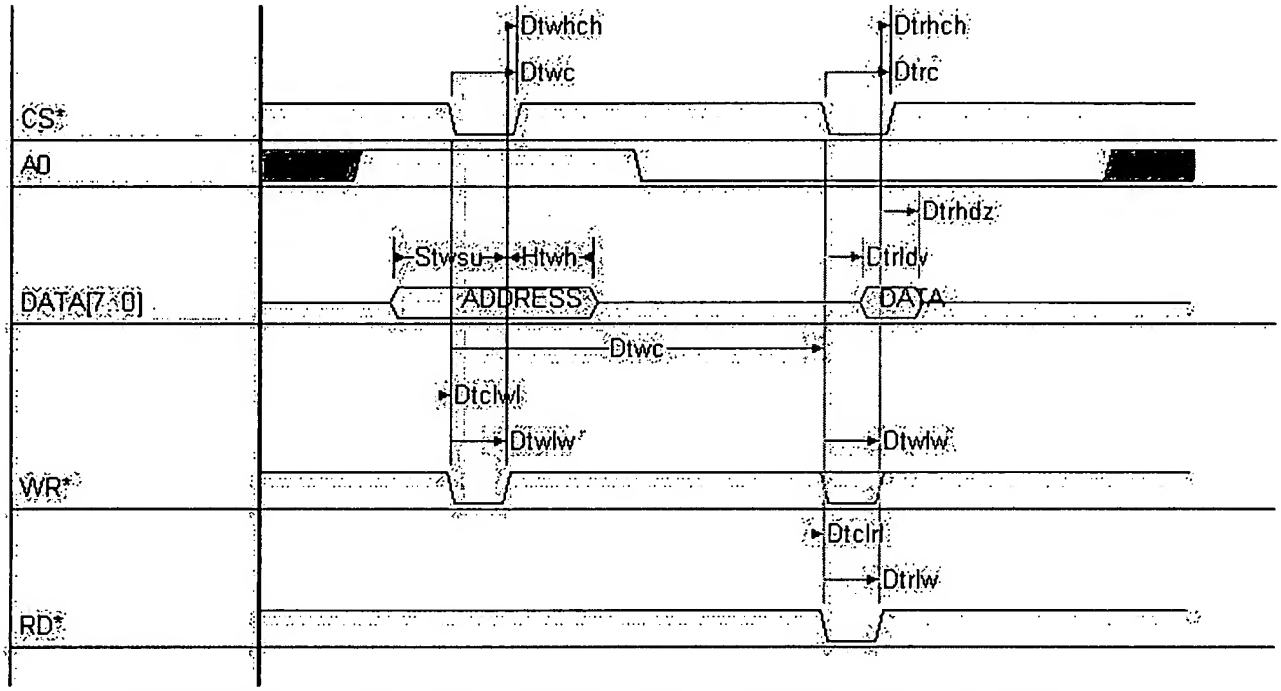
Electrical Specifications

Parameter	Typical	Unit	Condition
VCCIO Voltage range	3.0 – 5.2	V	
Logic input voltage	0 - 5.5	V	
Logic Input Threshold Low	0.8 max	V	
Logic Input Threshold High	2.4 min, 3 max	V	
Logic Output High	VCCIO-0.1 min	V	I = 100uA
	VCCIO-1 min	V	I = 4mA
Logic Output Low	0.4 max	V	I = 4mA
Output Short Circuit Current	+/-25	mA	
Output Disable leakage Current	+/-10	uA	Vout = VCC or 0V
Output Rise Time	4-20	ns	Cload = 50PF
Output Fall Time	4-20	ns	Cload = 50PF

Using the ALE signal, the Address and Data can be multiplexed through DATA[7..0] in a same bus cycle. The actual bus cycle with ALE is depicted as the following.



name	min	max	margin	comment
Dtalew	20		na (delay)	width of ALE high
Stavll	10		0	address valid to ALE low
Htllax		10	20	ALE low to address transition



In the non-ALE bus sequence, the address and data are clocked in separate bus cycles. The read bus sequence is depicted below. It is noted that the A0 signal is the now called CMD/DATA.

And the timing constraints are as follows:

name	min	max	margin	comment
Dtwlw	30		na (delay)	WR* low pulse width
Dtclwl	0		na (delay)	CS* low to WR* low
Stwsu	10		50	write data setup time
Dtwc	200		na (delay)	write cycle time
Htwh	10		36	write data hold time
Dtwhch	5		na (delay)	WR* high to CS* high
Dtrlw	30		na (delay)	read pulse width
Dtrc	200		na (delay)	read cycle time
Dtrhch	5		na (delay)	RD* high to CS* high
Dtclrl	0		na (delay)	CS* low to RD* low
Dtrldv		20	na (delay)	RD* low to data Valid
Dtrhdz		20	na (delay)	RD* high to data hi-z

The memory map is listed as the following:

FWE=0

Address	Register
00H	Mailbox 0
01H	Mailbox 1
02H	Mailbox 2
03H	Mailbox 3
04H	Mailbox 4
05H	Mailbox 5
06H	Mailbox 6
07H	Mailbox 7
08H	Interrupt Status
09H	Interrupt Mask
0AH	Status
0BH	CLK_OUT
0CH	CLR MB INT
0DH	CLR RTS INT
0EH	Decode Pwr OVRIDE
0FH	PWR Status
10H-FFH	reserved

FWE=1

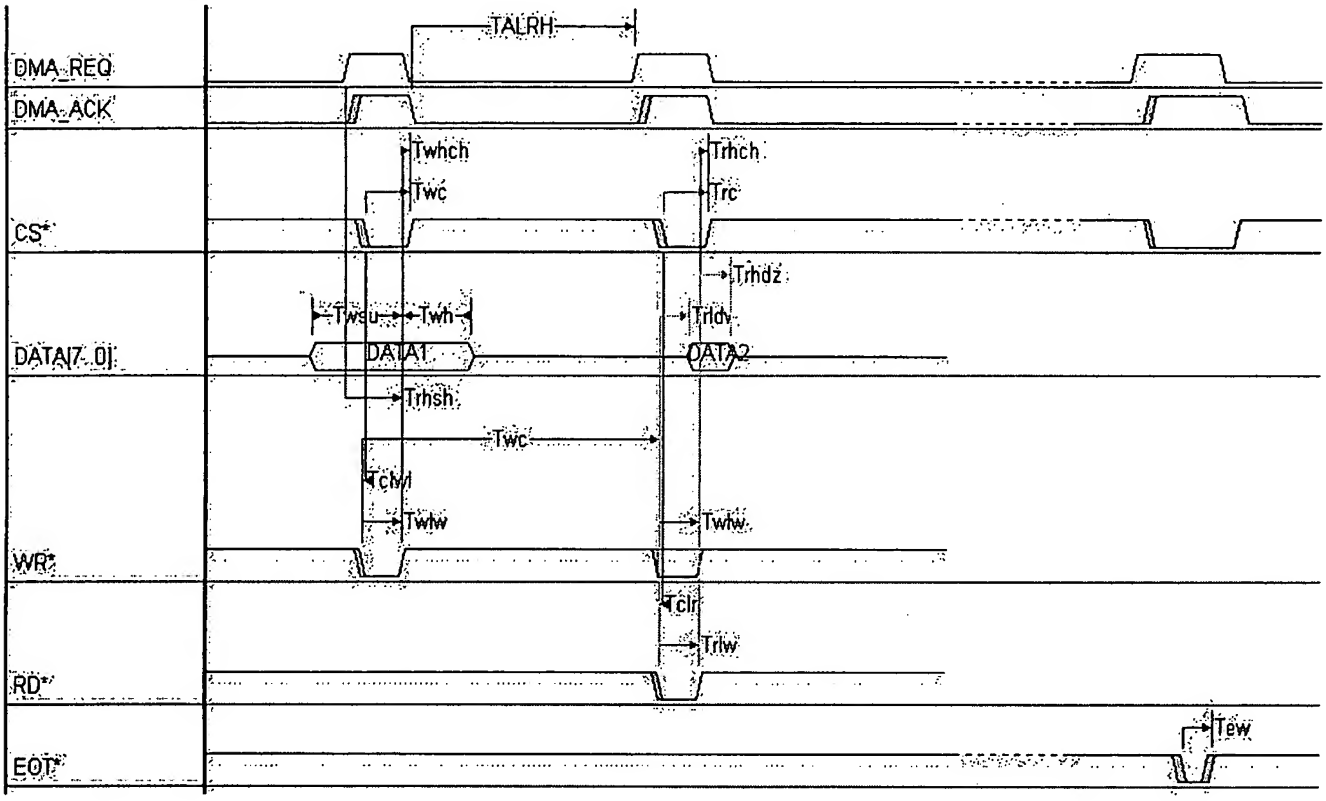
Address	Register
00H - 7FH	FLASH DATA
80H	Flash Page
81H	Flash Status
82H	Flash Error
83H	Flash Erase Mode
84H	Flash Erase
85H - FFH	reserved

DMA controller

The purpose of this DMA controller is to provide a high-speed data transfer channel between the USB FIFO and the external processor. Since DMA controllers allow the data to flow directly in or out of the

processor RAM, it eliminates the overhead incurred by the mailbox data transfer described in the previous section. This is essential for those applications that require Isochronous USB mode for data transfers, such as video applications. Upon data transfer, the DMA controller will handshake with the external DMA controller via its dedicated DMA_REQ and DMA_ACK signals. In order to simplify this DMA implementation, only the single cycle mode needs to be supported in this device. The DMA controller is controlled via the embedded micro only.

The timing diagram for the DMA is as following.



name	min	max	margin	comment
Twh	10		36	write data hold time
Twhch	5		na (delay)	WR* high to CS* high
Trlw	30		na (delay)	read pulse width
Trc	200		na (delay)	read cycle time
Trhch	5		na (delay)	RD* high to CS* high
Tclrl	0		na (delay)	CS* low to RD* low
Trldv		20	na (delay)	RD* low to data Valid
Trhdz		20	na (delay)	RD* high to data hi-z
Trhsh	100		na (delay)	Time Req High to Strobes High
Twc	200		na (delay)	write cycle time
TALRH	150		na (delay)	time from ack low to req high
Twlw	30		na (delay)	WR* low pulse width
Tew	20		na (delay)	time EOT pulse width

The following registers are used to set up the DMA controller. The address register is a 4-bit register with number 0 – 15 indicating the FIFO for end point 0 to 15. The count registers are 16 bit wide. The control register is used to commence the DMA transfer. Please be aware that the following registers are accessible only via the 8051 micro.

DMA ADDRESS REGISTER (R/W) ADDR: 9418H

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

DMA COUNT REGISTER MSB (R/W) ADDR: 9417H

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

DMA COUNT REGISTER LSB (R/W) ADDR: 9416H

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

DMA COTROL REGISTER (R/W) ADDR: 9419H

D7	D6	D5	D4	D3	D2	D1	D0
				INT EN	DMA DIR		DMA EN

DMA EN:	DMA enable	1: Start;	0: Stop (reset)
DMA DIR:	CLK_OUT enable	1: DMA write;	0: DMA read (out of RAM)
INT EN:	CLK_OUT enable	1: ENABLE;	0: DISABLE (reset)

Clock Generator

The clock generator shall be provided so that clock frequencies of 6, 12, 24 MHz can be programmed as output on CLKOUT. This clock output can be used as a clock source to the external micro-controller in a typical decoder application. **The clock frequency selection is performed via the bus interface.**

The electrical specification of CLKOUT is as follows:

Electrical Specifications

Parameter	Typical	Unit	Condition
*Duty Cycle	49-51	%	
Logic Input Threshold High	2.4 min	V	
Logic Output High	VCCIO-0.1 min	V	I = 100uA
	VCCIO-1 min	V	I = 4mA
Logic Output Low	0.4 max	V	I = 4mA
Output Short Circuit Current	+/-25	mA	
Output Disable leakage Current	+/-10	uA	Vout = VCC or 0V
Output Rise Time	4-20	nS	Cload = 50PF
Output Fall Time	4-20	nS	Cload = 50PF

Note: * this parameter is for the output rise/fall time symmetry.

CLK_OUT REGISTER (R/W) ADDR: 0x0B

D7	D6	D5	D4	D3	D2	D1	D0
CLK ENA						S1	S0

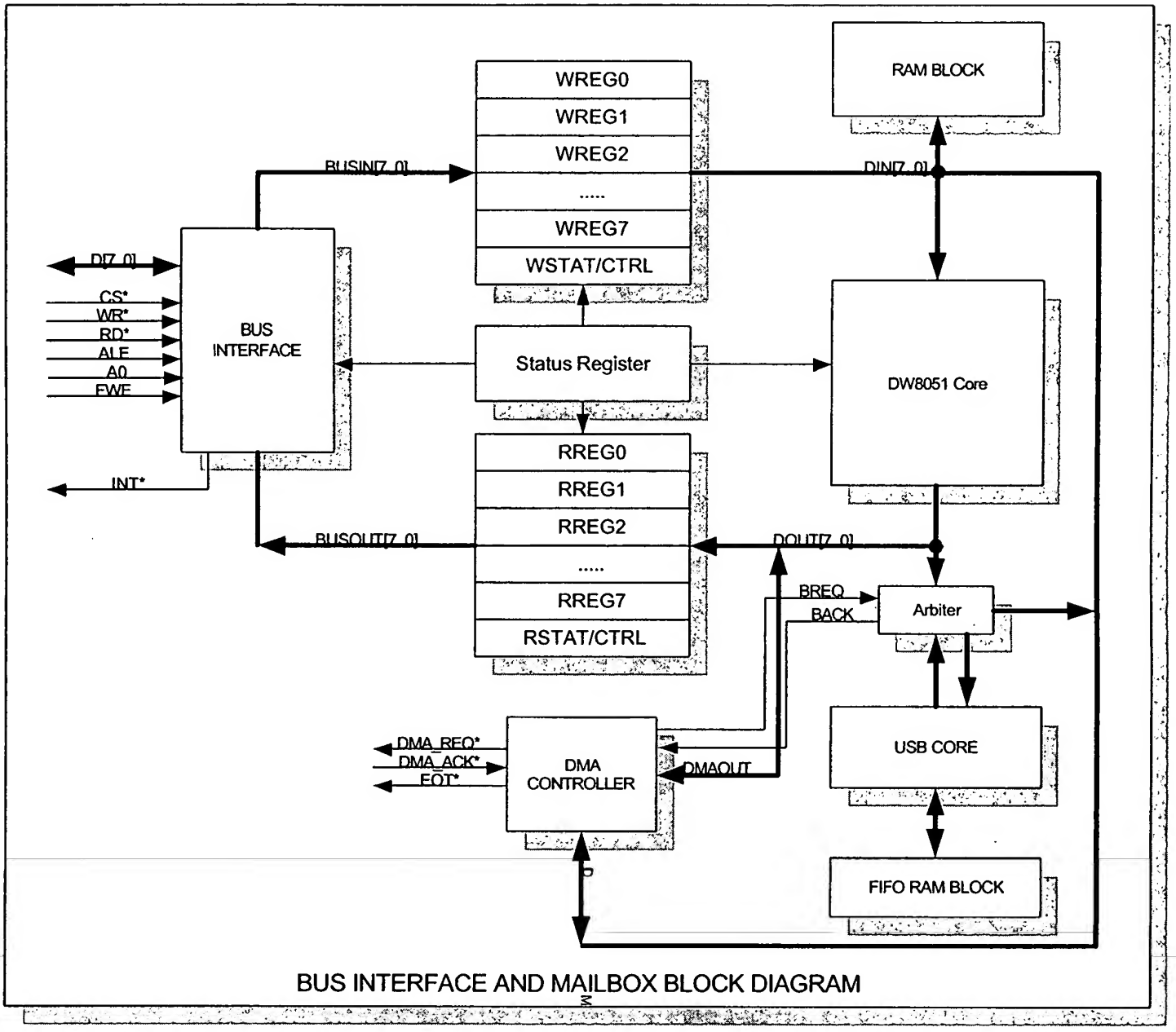
CLK ENA:	CLK_OUT enable	1: ENABLE (reset); 0: DISABLE
S1 – S0:	0: 6MHz(reset); 1: 12MHz; 2: 24MHz	

The (reset) next to the state indicates the default setting after RESET.

Mailbox I/O block

The diagram labeled "BUS INTERFACE AND MAILBOX DIAGRAM" depicts the basic architecture of the mailbox I/O block. The mailbox is designed to facilitate the command and data transfer between the external processor and the embedded 8051 micro. Although the read and write to the mail boxes are sharing the same address, there are physically two separate sets of eight registers dedicated to the input and the output mail boxes as noted WREG(0-7) and RREG(0-7) in the following diagram. Interrupts shall be generated upon the writing and the reading of register 7. The writing of WREG7 will cause the interrupt to the 8051, where as the reading of WREG 7 via 8051 will cause interrupt being generated to the external processor. Both the buffer full and empty interrupt shall be made programmable via processor control as described later in this section. The status register shall be made available to both sides. In addition, there shall be a semaphore available for each side to signal its readiness. This shall be done via the standard interface without added extra I/O pins. They are called the MB_RTS and MB_CTS hereafter to avoid any confusion. The 8051 processor owns the MB_RTS, where as the MB_CTS does the external scanner processor control. There are two registers set aside to clear the Mailbox interrupt and CTS interrupts.

Since the power to the external scanner is controlled via the 8051, the power status of this chip can be monitored by the external micro via the power status register. This power status register contains not only the power status of the scanner but also the PLL on/off status of this chip. There will be another register to allow the external micro to prohibit the 8051 from removing its power. The detail description of the power state and control registers will be in the Wake Up and Power Control section of this document.



BUS INTERFACE AND MAILBOX BLOCK DIAGRAM

MAILBOX INTERRUPT CONTROL (8051) REGISTER (R/W) ADDR: 9409h

D7	D6	D5	D4	D3	D2	D1	D0
WREG[1] FULL	RREG[1] EMTY	CTS EVENT				PULSE INT	INT POL

WREG FULL: interrupt on WREG filled by ext. proc. 1: enabled 0: disabled;
RREG EMPTY: interrupt on RREG emptied by ext. proc. 1: enabled 0: disabled;
CTS EVENT: MB_CTS event interrupt 1: enabled 0: disabled;
PLUSE INT: PULSE interrupt or LEVEL interrupt 1: PULSE 0: LEVEL;
INT POL: interrupt signal polarity 1: active high 0: active low;

MAILBOX INTERRUPT STATUS (8051) REGISTER (R) ADDR: 940Ah

D7	D6	D5	D4	D3	D2	D1	D0
WREG[1] FULL	RREG[1] EMTY	CTS INT					

WREG FULL: flag signals the WREG full event 1: buffer filled 0: nothing;
RREG EMPTY: flag signals the RREG empty event 1: buffer emptied 0: nothing;
CTS INT: MB_CTS event interrupt 1: Event occurred 0: nothing;

Note: Reading this register will clear the event status (e.g. RREG full or WREG empty).

MAILBOX INTERRUPT CONTROL (EXTERNAL) REGISTER (R/W) ADDR: 09H

D7	D6	D5	D4	D3	D2	D1	D0
RREG[1] FULL	WREG[1] EMTY	RTS EVENT				PULSE INT	INT POL

RREG FULL: interrupt on RREG filled by MIA's 8051 1: enabled 0: disabled;
WREG EMPTY: interrupt on WREG emptied by MIA's 8051 1: enabled 0: disabled;
RTS EVENT: MB_RTS event interrupt 1: enabled 0: disabled;
PLUSE INT: PULSE interrupt or LEVEL interrupt 1: PULSE 0: LEVEL;
INT POL: interrupt signal polarity 1: active high 0: active low;

MAILBOX INTERRUPT STATUS (EXTERNAL) REGISTER (R) ADDR: 08H

D7	D6	D5	D4	D3	D2	D1	D0
RREG[1] FULL	WREG[1] EMTY	RTS INT					

RREG FULL: flag signals the RREG full event 1: buffer filled 0: nothing;
WREG EMPTY: flag signals the WREG empty event 1: buffer emptied 0: nothing;
RTS INT: flag signals the MB_RTS event interrupt 1: Event occurred 0: nothing;

Note: Reading this register will clear the event status (e.g. RREG full or WREG empty).

MAILBOX STATUS (EXTERNAL/INTERNAL) REGISTER (R/W) ADDR: 0AH/9408h

D7	D6	D5	D4	D3	D2	D1	D0
RREG[1] FL/RD	WREG[1] FL/RD	RTS[2] FLAG	CTS[3] FLAG				

RREG FL/RD : flag set to '1' when the RREG is filled and clear to '0' when the RREG is emptied;
WREG FL/RD: flag set to '1' when the WREG is filled and clear to '0' when the WREG is emptied;
RTS FLAG: RTS flag is set or reset by the 8051 1: set 0: reset;
CTS FLAG: CTS flag is set or reset by the external processor 1: set 0: reset;

MAILBOX (EXTERNAL/INTERNAL) REGISTER 0-7 (W/R) ADDR: 00-08H/9400-9408h

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

Note: [1] Both the FULL and EMPTY interrupts or status are modified upon the writing and reading of the 7th register of either WREG or RREG.

[2] Only the RTS FLAG can be written by the MIA's 8051 process with a '1' or '0'. Writing to other bits of this register has no effects on them.

[3] Only the CTS FLAG can be written by the external process with a '1' or '0'. Writing to other bits of this register has no effects on them.

There are two physical banks of mailbox registers, however, the reading and writing of registers are pertaining to the perspective incoming and outgoing mail registers. For example, the internal 8051 processor can only write to RREG0-7 and read from WREG0-7, where as the external processor only writes to the WREG0-7 and reads from the RREG0-7.

FLASH ROM/Static RAM

The total amount of program space in the FLASH ROM shall be 32Kilo-bytes. The FLASH block shall be partitioned into 128-byte erasable sectors. The device shall provide required FLASH programming voltages so that In-System-Programmability is available without additional supply voltages other than the prime voltage (+5VDC). The FLASH shall guarantee at least ten thousand (10,000) reprogramming cycles.

There should be 2K bytes of Static RAM embedded in this device in addition to the 256-byte scratch pad for the 8051. Both ROM and RAM shall be setup for byte-wide (8-bit) access. The read access time for FLASH ROM shall be no worse than 80ns and no worse than 20ns for SRAM read/write accesses.

FLASH ROM programming

The programming of this embedded FLASH will be designed without micro intervention, which would otherwise require additional RAM to facilitate the FLASH load. The underlying FLASH programming method reflects a generic FLASH device programming. Upon detecting the FLASH WRITE (via FWE signal), the device will enter its FLASH memory mode. Meanwhile, the embedded micro will relinquish control of all buses and hold itself in reset state. The local controller can then access the embedded FLASH blocks as if it is a passive memory device. In order for the local controller to communicate with an external host during FLASH programming, the TXD and RXD will be bypassed to the local controller. The full 32K of FLASH block is divided into 256 of 128 byte sectors. This arrangement is to work around the limitation of using the 8-bit bus. Conjoining both the PAGE register and the offset of the seven LSB bits from the address makes up the actual address to the FLASH memory. Once the PAGE register is set, subsequent access will be made to the page locations offset by the ADDRESS latch (refer to bus interface for ADDRESS latch). It is important to remember that the following registers are only visible while Flash Write Enable (FWE) is active.

FLASH DATA REGISTER (R/W) ADDR: 0-7FH

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7-D0: the 8 bit that gets write/read from the flash. The actual FLASH address is made up of the page register and the address, which are fifteen bits total.

FLASH PA GE/SECTOR REGISTER (R/W) ADDR: 80H

D7	D6	D5	D4	D3	D2	D1	D0
P7	P6	P5	P4	P3	P2	P1	P0

P7-P0: the 8-bit sector number of the FLASH memory address. Each sector contains 128 bytes. And there are total of 256 sectors.

FLASH STATUS REGISTER (R) ADDR: 81H

D7	D6	D5	D4	D3	D2	D1	D0
FAE							FM_ RDY

FAE: Flash Access Error, indicates attempting to access Flash while busing programming or erasing, active high.

FM_RDY: 1: Ready 0: Busy

FLASH ERROR REGISTER (R) ADDR: 82H

D7	D6	D5	D4	D3	D2	D1	D0
SFC						UEC	UWC

SFC: Successful Flash Command, after complete erase or program command, active high.

UEC: Unsuccessful Erase Command that indicates not all bits became a '0' after erase command, active high.

UWC: Unsuccessful Write Command that indicates not all bits became a '0' after erase command, active high.

FLASH ERASE MODE REGISTER (R/W) ADDR: 83H

D7	D6	D5	D4	D3	D2	D1	D0
						M1	M0

M1-M0: 00 – invalid erase mode
01 – sector erase (128 bytes)
10 – page erase (2K bytes)
11 – block erase (32K bytes)

The page or sector address resides in the PAGE/SECTOR register.

FLASH ERASE REGISTER (W) ADDR: 84H

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	1	0	1	0

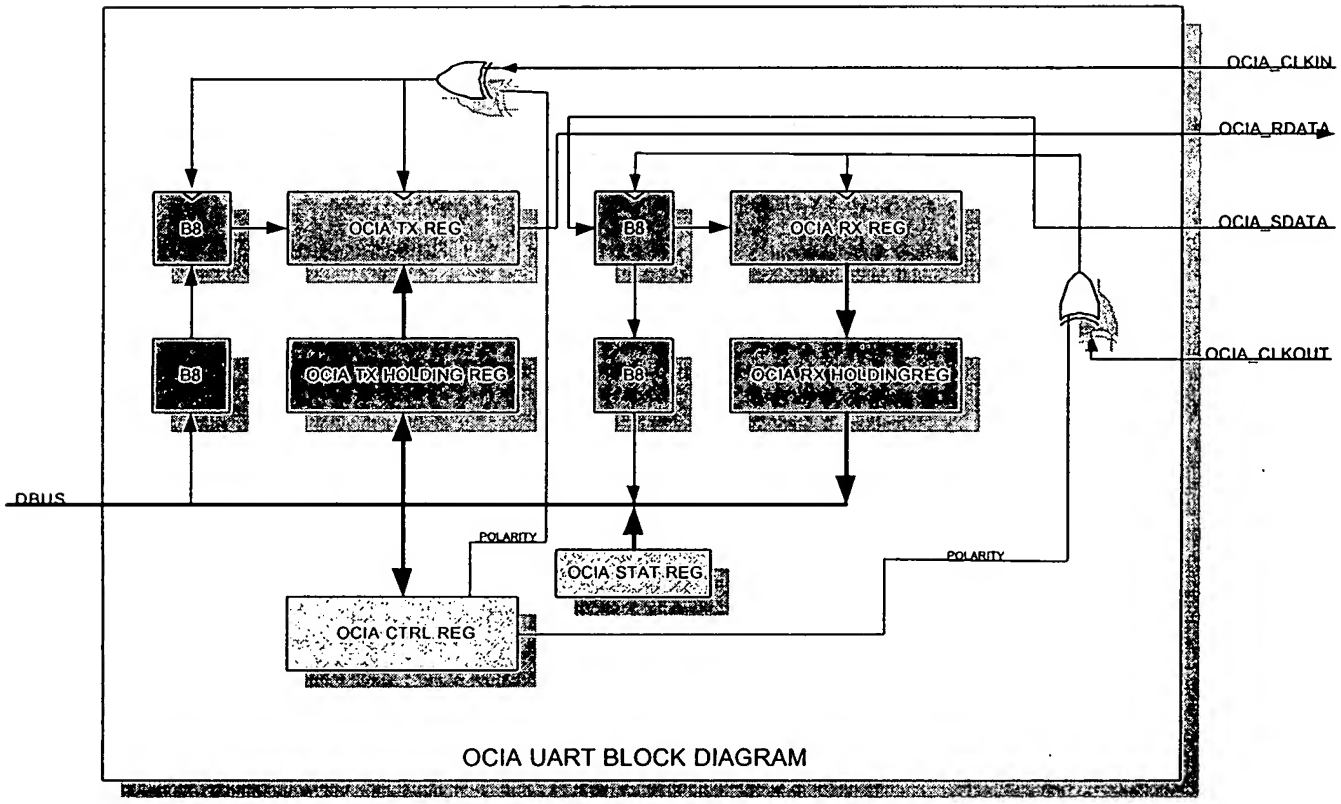
This register is used to generate an erase strobe to the FLASH memory. The erase mode is determined by the content of the ERASE MODE register. In order to prevent inadvertent erasures, the data content has to be 55H. Data value of other than 55H shall be writing to the same register after the Erase is finished.

UART

The UART shall support at the minimum the following baud rates: 110, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 187500 (only for RS-485) BPS. For the 8051 processor, Timer 2 shall be provided as baud rate generator. With a 24MHz CPU clock, timer 2 will use the 12MHz clock (8051 CPU clock divided by 2) and use it to generate the required 16x-baud rate clock for the UART. The timer 2 shall also be able to use the external (T2 input) clock input so that 115.2K and 38.4K baud can be generated using the external 1.8461MHz clock. The UART shall have parity generation functionality for both transmission and receiving as an instrument for error detection. It shall also detect parity and overrun errors.

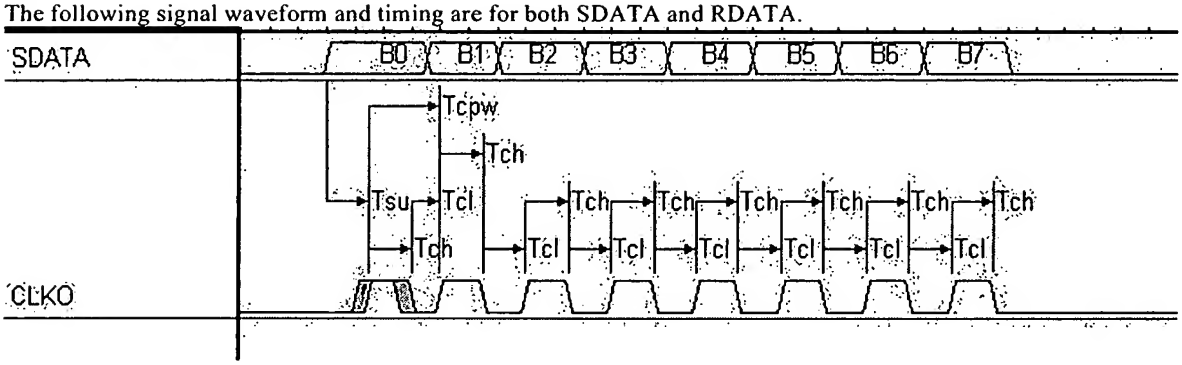
OCIA

The OCIA is a full duplex synchronous serial interface with dedicated clock and data for each data direction. Its clock rate is typical 300Kilo Hertz. With its full duplex implementation, the OCIA consists of three input signals and one output signal. The CLKOUT and SDATA pair is used to transmit data from the host into the ASIC, where as the CLKIN and SDATA pair is to output data to the host. Both the input and output data shall support the 8bit (S-format) as well as the 9bit (F-format) OCIA data formats. Registers such as control, status and data shall be implemented for this interface. Within the control register, programmability such as 8/9 bits data, polarity selection on both in and out clocks shall be provided. Since the transmit data stream (RDATA) will start with a ready bit first, this would extend an 8/9 bit data to 9/10 bits. The following block diagram illustrates its overall configuration. Digital filtering technique shall be implemented to eliminate noise on both the CLKI and CLKO signal lines. During it application, the OCIA_RDATA signal is normally connected to an open drain transistor, whereas the rest of the signals are outputs from CMOS receivers. Therefore, signal inversion is not required designing with this ASIC. The waveform diagram in the following pages illustrates the signal timing requirements. It should be noted that the required optical couplers are not enclosed in this ASIC. External optical couplers have to be used to complete the OCIA interface design. The RDATA output consists of an open drain transistor that can sink up to 5mA and can possibly drive an optical coupler directly. Otherwise, an external drive device, such as transistor, must be used.

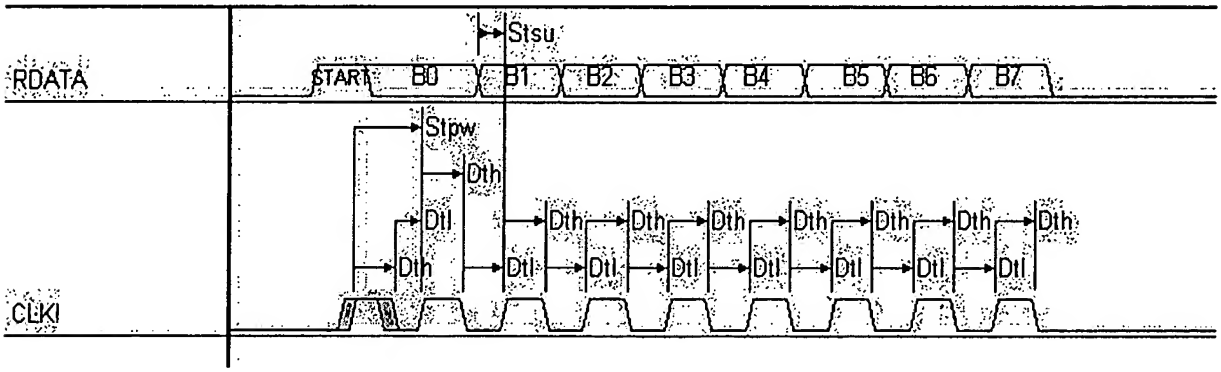


OCIA UART BLOCK DIAGRAM

The following signal waveform and timing are for both SDATA and RDATA.



name	min	max	margin	comment
Tch	1500		na (delay)	time clock high
Tcl	1500		na (delay)	time clock low
Tcpw	3000		na (delay)	clock pulse width
Tsu	1000		na (delay)	data setup time



name	min	max	margin	comments
Dth	1500		na (delay)	pulse width clock high
Dtl	1500		na (delay)	pulse width clock low
Stpw	3000		na (delay)	clock pulse width
Stsu	1000		0	

The simplified control and clock out control registers are defined as the following:

OCIA CONTROL REGISTER (R/W) ADDR: 9410h

D7	D6	D5	D4	D3	D2	D1	D0
CLKI POL	CLKO POL	RX INT	TX INT		SHORT /EXT	RX ENA	TX ENA

CLKI POL:	1 – clock on rising-edge	0 – clock on falling-edge (reset)
CLKO POL:	1 – clock on rising-edge	0 – clock on falling-edge (reset)
SHORT/$\overline{\text{EXT}}$:	1 – 8 bit (reset)	0 – 9 bit extended mode
RX ENA:	1 – receive enabled	0 – receive disabled (reset)
TX ENA:	1 – transmit enabled	0 – transmit disabled (reset)
RX INT :	1 – RX interrupt enabled	0 – RX interrupt disabled (reset)
TX INT:	1 – TX interrupt enabled	0 – TX interrupt disabled (reset)

Both the RX and TX interrupt will be generated as edge sensitive interrupts. In other word, the DR interrupt will only be generated upon the data received. The Transmit Buffer Empty interrupt will consequently be generated on the instance when the buffer becomes empty.

OCIA STATUS REGISTER (R) ADDR: 9411h

D7	D6	D5	D4	D3	D2	D1	D0
INT FLAG						DR	TB EMPT

INT FLAG:	1 – interrupt generated	0 – no interrupt
DR:	1 – Data received	0 – no data (reset)
TB EMPT:	1 – transmit buffer empty (reset)	0 – transmit buffer not empty

Reading this register will clear the INT FLAG bit, where as reading data receive register will clear the DR flag.

OCIA TRANSMIT DATA REGISTER LSB (R/W) ADDR: 9412h

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

OCIA TRANSMIT DATA REGISTER MSB (R/W) ADDR: 9413h

D7	D6	D5	D4	D3	D2	D1	D0
							D8

The OCIA TDR MSB is only valid on 9 bit transmission.

OCIA RECEIVE DATA REGISTER LSB (R/W) ADDR: 9414h

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

OCIA RECEIVE DATA REGISTER MSB (R/W) ADDR: 9415h

D7	D6	D5	D4	D3	D2	D1	D0
							D8

The OCIA RDR MSB is only valid on 9 bit transmission.

Programmable Interval Timer

The timer0-2 should be made available as a standard 8051 processor.

Watch Dog Timer

The watch dog timer can be used to generate either an interval interrupt or to reset the micro in the case that the micro failed to refresh the watch dog timer. Both the interrupt and CPU reset are generated upon counter overflow. The WDT is an up count only counter and it will generate interrupt or reset when the counts overflow (from FFH to 00H) occurs. There are two registers associated with this WDT, the WDT control/status register and write-only WDT register.

WDT CONTROL/STATUS REGISTER (R/W) ADDR: 940Ch

D7	D6	D5	D4	D3	D2	D1	D0
WDT	OVR	INT		RUN /$\overline{\text{STOP}}$	S2	S1	S0

WDT: 1 – watch-dog timer mode 0 – internal timer mode (reset)

OVR: read only – overflow indicator, reset after read

INT: 1 – interrupt enable

RUN/$\overline{\text{STOP}}$: 1 – Run 0 – Stop (reset)

S2-S0: clock selection

0 0 0	:	3.3 µs (reset)	300khz
0 0 1	:	13.2 µs	300k/4
0 1 0	:	52.8 µs	300k/16
0 1 1	:	211.2 µs	300k/64
1 0 0	:	1.69 ms	300k/512
1 0 1	:	13.5 ms	300k/4096
1 1 0	:	54.1 ms	300k/16384
1 1 1	:	216.2 ms	300k/65536

WDT REGISTER (W) ADDR: 940Dh

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0

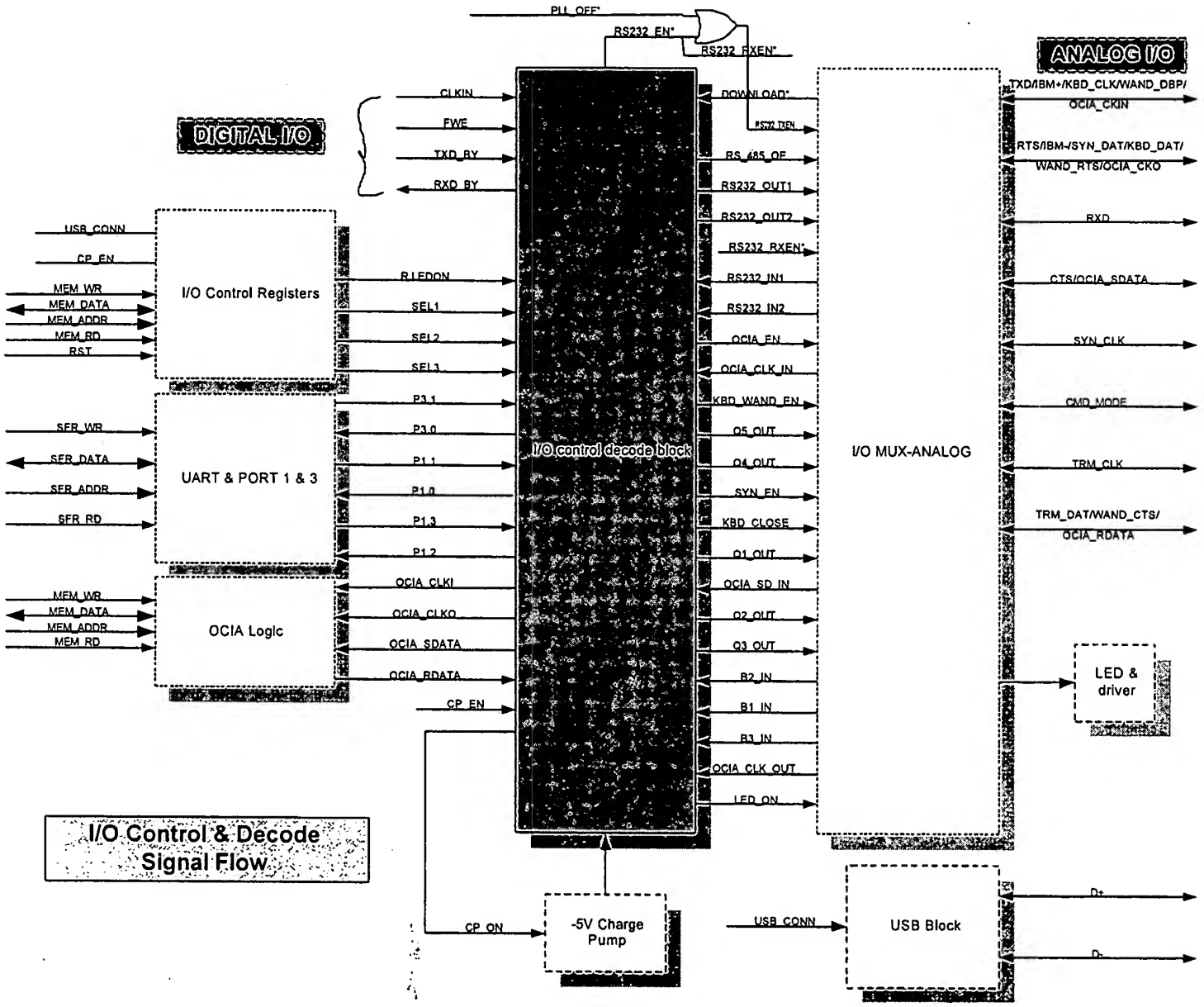
USB Control and Configuration

This section defines the USB SIE to micro interface. There are numerous control and status registers that are dedicated to the USB function. Control registers shall include general control, endpoint control, address register, interrupt control and error (stall) generation. Status registers shall contain general status, error status, interrupt status and frame number register.

The definitions of the above registers are outlined in the Inventra MUSBFSFC production specification and user's guide. The base address of the USB block is at 8800h.

I/O Control Logic Block

The I/O Control Logic and its related signal flow are depicted in the next diagram.


PLL_OFF*
RS232_EN*
RS232_RXEN*
ANALOG I/O
DIGITAL I/O
CLKIN
FWE
TXD_BY
RXD_BY
DOWNLOAD*
RS232_TXEN
RS_485_OE
RS232_OUT1
RS232_OUT2
RS232_RXEN*
RS232_IN1
RS232_IN2
OCIA_EN
OCIA_CLK_IN
KBD_WAND_EN
O5_OUT
O4_OUT
SYN_EN
KBD_CLOSE
O1_OUT
OCIA_SD_IN
O2_OUT
O3_OUT
B2_IN
B1_IN
B3_IN
OCIA_CLK_OUT
LED_ON
TXD/IBM+/KBD_CLK/WAND_DBP/
OCIA_CKIN
RTS/IBM-/SYN_DAT/KBD_DAT/
WAND_RTS/OCIA_CKO
RXD
CTS/OCIA_SDATA
SYN_CLK
CMD_MODE
TRM_CLK
TRM_DAT/WAND_CTS/
OCIA_RDATA
USB_CONN
CP_EN
MEM_WR
MEM_DATA
MEM_ADDR
MEM_RD
RST
I/O Control Registers
R_LEDON
SEL1
SEL2
SEL3
P3.1
P3.0
P1.1
P1.0
P1.3
P1.2
OCIA_CLKI
OCIA_CLKO
OCIA_SDATA
OCIA_RDATA
SFR_WR
SFR_DATA
SFR_ADDR
SFR_RD
UART & PORT 1 & 3
MEM_WR
MEM_DATA
MEM_ADDR
MEM_RD
OCIA Logic
I/O control decode block
I/O MUX-ANALOG
LED &
driver
I/O Control & Decode
Signal Flow
CP_ON
-5V Charge
Pump
USB_CONN
USB Block
D+
D-

Truth table of I/O interface controls

DOWN LOAD*	F.WE	S2	S1	S0	OCIA_EN	RS_485_OE	RS_232_EN*	KBD_CLOSE	KBD_WAND_EN	SYN_EN	RS232_OUT1	RS232_OUT2	Q1_OUT	Q2_OUT	Q3_OUT	Q4_OUT	Q5_OUT	LED_ON	RXD_BY	P3.0	P3.5	P3.4	OCIA_CLKI	OCIA_CLKO	OCIA_RDATA	Comments
1	0	0	0	0	1	0	1	0	0	0	1	1	OCIA_RDATA	0	0	0	0	R.LEDON	1	1	0	0	OCIA_CLK_IN	OCIA_CLK_OUT	OCIA_SD_IN	OCIA
1	0	0	0	1	0	0	0	0	0	0	P3.1	P1.1	0	0	0	0	0	R.LEDON	1	RS232_IN1	RS23_IN2	0	0	0	0	RS-232
1	0	0	1	0	0	0	1	0	1	0	1	1	P1.1	P1.6	0	0	1	R.LEDON	1	1	B1_IN	B2_IN	0	0	0	KBD_OPEN
1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	R.LEDON	1	1	B1_IN	B2_IN	0	0	0	KBD_CLOSE
1	0	1	0	0	0	0	1	0	0	1	1	1	0	0	P1.1	P1.6	0	R.LEDON	1	1	B3_IN	OCIA_CLK_OUT	0	0	0	SYNAPSE
1	0	1	0	1	0	1	1	0	0	0	P3.1	1	0	0	0	0	0	R.LEDON	1	OCIA_CLK_IN	0	0	0	0	0	IBM_XMTR
1	0	1	1	0	0	0	1	0	0	0	P3.1	1	0	0	0	0	0	R.LEDON	1	OCIA_CLK_IN	0	0	0	0	0	IBM_RCVR
1	0	1	1	1	0	0	1	0	1	1	1	1	0	0	0	P1.6	P1.1	R.LEDON	1	1	B1_IN	0	0	0	0	WAND_EMUL
0	X	X	X	X	0	0	0	0	0	0	TXD_BY	1	0	0	0	0	0	R.LEDON	RS232_IN1	1	0	0	0	0	0	download
1	1	X	X	X	0	0	1	0	0	0	1	1	0	0	0	0	0	R.LEDON	1	1	0	0	0	0	0	FLASH WRITE no download

X: don't care

Interface Control

The interface selection, LED on/off, USB_CONN, RES_IN and charge pump enable are controlled through this functional block. The interface control register is detailed in the following.

INTERFACE CONTROL REGISTER (R/W) ADDR: 940Bh

D7	D6	D5	D4	D3	D2	D1	D0
CP_ ON	USB_ Conn	LED_ ON	RES_ IN		SE3	SE2	SE1

CP_ON:	-5V charge pump ON	1: ON	0: OFF	reset: ON
USB_Conn:	Control the 1.5K PU RES.	1: IN	0: OUT	reset: OUT
LED_ON:	debug LED on/off ctrl	1: ON	0: OFF	reset: OFF
RES_IN:	pull-up resistors	1: IN	0: OUT	reset: OUT

SE3-SE1:

0 0 0	:	OCIA
0 0 1	:	RS-232
0 1 0	:	Keyboard Wedge - Open
0 1 1	:	Keyboard Wedge - Close
1 0 0	:	Synapse
1 0 1	:	IBM Send
1 1 0	:	IBM Receive
1 1 1	:	WAND Emulation

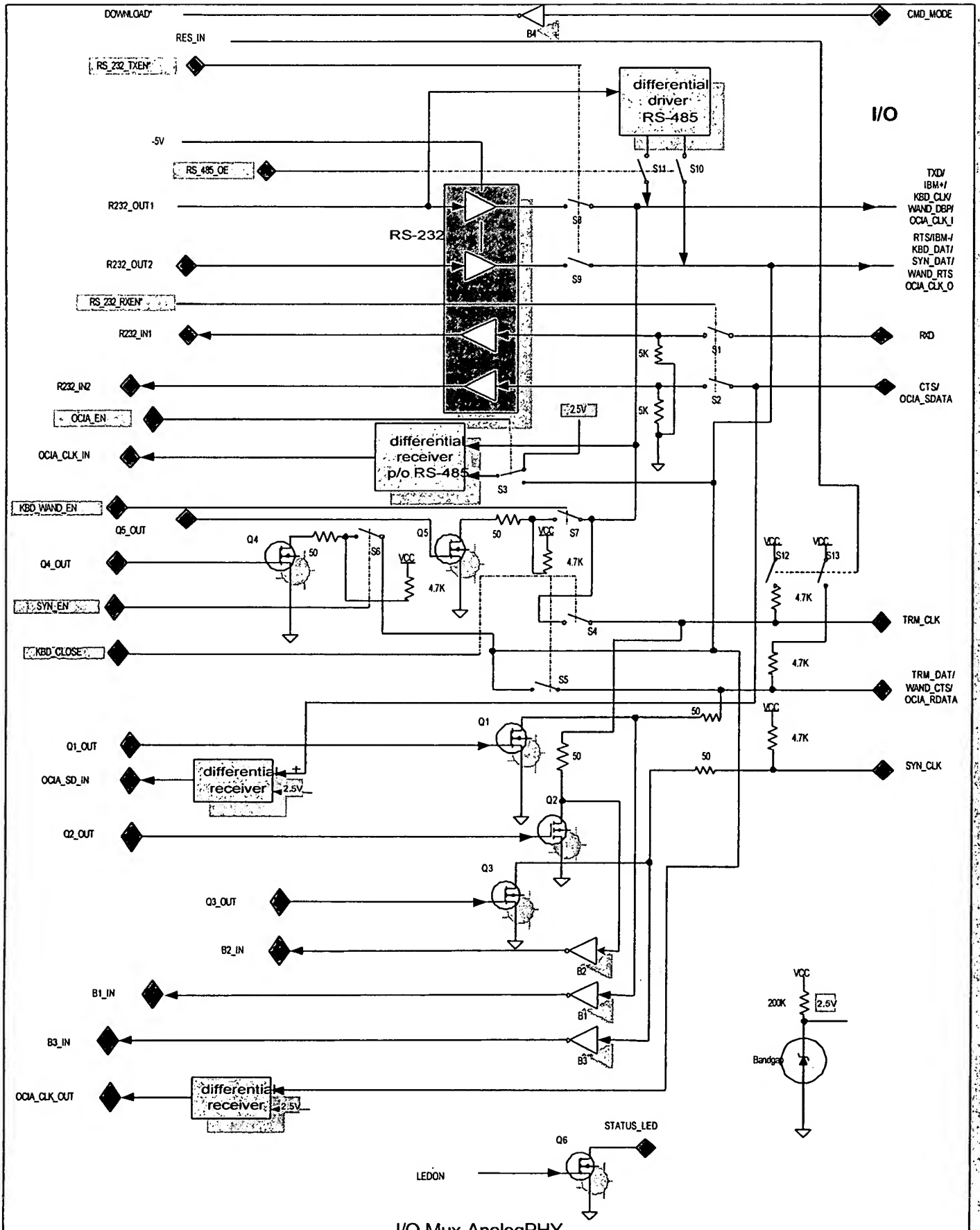
Interface decode logic

This interface decode logic is used to multiplex 8051 port pins to the appropriate I/O control signals in the analog I/O block. This block is also responsible for turning on or off appropriate analog switches upon I/O interface selection. Besides these interface selection input signals, SELx, Flash Write Enable and the download flag are all govern the outputs from this block. For example, the download enable will force the TXD and RXD of RS232 to bypass the internal processor. The overall decode truth table is listed in the previous page.

I/O Mux-Analog PHY

The I/O Mux-Analog block is illustrated on the next page. This analog section includes various physical I/O circuits. There will be only one I/O interface enabled at a time. The switches were designed in to permit multiplexing of all the different interface signals. The USB D+ and D- and TRM_CLK and TRM_DAT have their dedicated I/O pads in the chip. Ultimately, these signals may be sharing I/O connections with other I/O signals, such as RXD and CTS, due to the limited I/O pins available on a standard connector used by Symbol. Therefore, the following signals have to be made ±5V tolerant.

1. RXD
2. CTS /OCIA_SDATA
3. D+
4. D-
5. TRM_CLK
6. TRM_DAT/WAND_CTS/OCIA_RDATA


DOWNLOAD*
RES_IN
RS_232_TXEN*
-5V
RS_485_OE
R232_OUT1
R232_OUT2
RS_232_RXEN*
R232_IN1
R232_IN2
OCIA_EN
OCIA_CLK_IN
KBD_WAND_EN
Q5_OUT
Q4_OUT
SYN_EN
KBD_CLOSE
Q1_OUT
OCIA_SD_IN
Q2_OUT
Q3_OUT
B2_IN
B1_IN
B3_IN
OCIA_CLK_OUT
LEDON
STATUS_LED
B4
CMD_MODE
differential driver RS-485
I/O
S11
S10
RS-232
S8
S9
TXD/ IBM+/ KBD_CLK/ WAND_DBP/ OCIA_CLK_I
RTS/IBM-/ KBD_DAT/ SYN_DAT/ WAND_RTS OCIA_CLK_O
S1
S2
RXD
CTS/ OCIA_SDATA
5K
2.5V
differential receiver p/o RS-485
S3
50
VCC
S7
4.7K
Q4
Q5
S6
S12
S13
TRM_CLK
S4
TRM_DAT/ WAND_CTS/ OCIA_RDATA
S5
Q1
Q2
Q3
differential receiver
SYN_CLK
200K
Bandgap
Q6
I/O Mux-AnalogPHY

The enable control signal to each of the above I/O switches are as following:

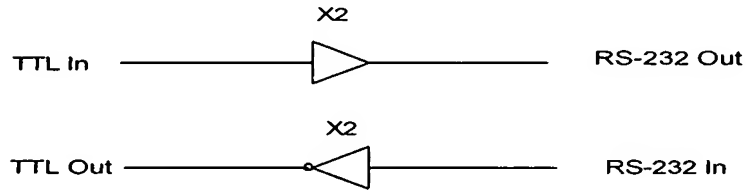
RS_485_OE:	'1' or logic high shall close S10 and S11. '0' or logic low shall open make S10 and S11 open.
RS_232_RXEN*:	'1' or logic low shall open S1 and S2. '0' or logic high shall close S1 and S2.
RS_232_TXEN*:	'1' or logic low shall open S8 and S9. '0' or logic high shall close S8 and S9.
OCIA_EN:	'1' or logic high shall switch S3 to its upper position. '0' or logic low shall switch S3 to its lower position.
KBD_WAND_EN:	'1' or logic low shall close S7. '0' or logic high shall open S7.
SYN_EN:	'1' or logic low shall close S6. '0' or logic high shall open S6.
KBD_CLOSE:	'1' or logic low shall close S4, S5. '0' or logic high shall open S4, S5.
RES_IN:	'1' or logic low shall close S12. '0' or logic high shall open S12.

The required I/O signals for each interface is:

OCIA:
OCIA_CLK_IN, OCIA_RD_IN, OCIA_CLK_OUT
RS-232:
RS232_OUT1, RS232_OUT2, RS232_IN1, RS232_IN2
KEYBOARD WEDGE:
B1_IN, B2_IN, Q1_OUT, Q2_OUT, Q5_OUT
SYNAPSE:
OCIA_CLK_OUT, B3_IN, Q3_OUT, Q4_OUT
IBM 468x:
RS232_OUT1, OCIA_CLK_IN
WAND EMULATION:
B1_IN, Q4_OUT, Q5_OUT

RS-232 I/O specification

This specification applies whenever the I/O signals are configured to be in RS-232 mode. Any detail not specified herein shall be defaulted to EIA/TIA-232E specification. The speed of serial transmission shall be no less than 120kilo-Bits-Per-Second. There are two transmit signals, TXD and RTS, and two receive signals, RXD and CTS. The output disable shall be provided so that these output pins can be shared among other functions.



Electrical Specifications

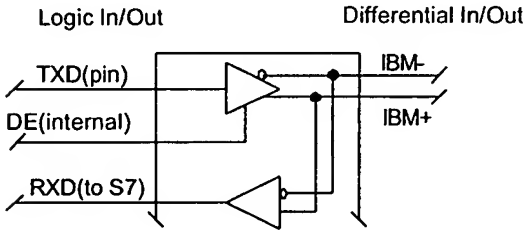
Parameter	Typical	Unit	Condition
RS-232 output voltage swing	+/-4.2	V	Vcc = 5V, Rload = 3K Ohm
RS-232 output resistance	300 min	Ohm	Vcc = 0V, Vout = +/-2V
Slew Rate	4-30	V/us	Rload = 3K Cload = 1000PF, +3V to -3V
(note 1)Input Logic Threshold Low	0.8 max	V	
(note 1)Input Logic Threshold High	2.4 min	V	
(note 1)Logic Output High	3.7 min	V	VCC = 5V
(note 1)Logic Output Low	0.1 max	V	I = 10uA
RS-232 Input voltage range	+/-5	V	
RS-232 Input Threshold high	2.6 max	V	
RS-232 Input Threshold low	0.8 min	V	
RS-232 Input Hysteresis	0.2	V	
RS-232 Input Resistance	3K-7K	Ohm	
Baud Rate	120K	BPS	Rload = 3K Cload = 1000PF
Output Short Circuit Current	+/-25	mA	
Output Disable leakage Current	+/-10	uA	Rload = 54 Ohm, VCC=5.0V

Note: 1. Specifications are for simulation only.

RS-485 I/O specification

This specification applies whenever the I/O is configured to be in RS-485 mode. Any detail not specified herein shall be defaulted to the EIA/TIA-485E specification. This function shall provide a pair of differential signals for both transmitter and receiver as depicted in the next diagram. The output-enable control signal, DE, is an internally derived interface control function.

Pin Name Definitions



RXD: Receiver Output
DE: Data Drive Enable from logic decoder
TXD: Data In
IBM+/-: Differential Input/Output, which are denoted as A and B in the next two tables

Truth Table (Output)

TXD	DE	A	B
X	0	Hi-Z	Hi-Z
0	1	0	1
1	1	1	0

X: don't care Hi-Z : high-impedance

Truth Table (Input)

A,B	RXD
A>B+0.2	1
B>A+0.2	0
input open	1

Electrical Specifications

Parameter	Typical	Unit	Condition
Differential Drive Output	2 min	V	Rload = 100 Ohm, VCC=5.0V
	1.5 min	V	Rload = 54 Ohm, VCC=5.0V
Output Common-Mode Voltage	3 max	V	Rload = 54 Ohm, VCC=5.0V
Output Disable leakage Current	+/-10	uA	Rload = 54 Ohm, VCC=5.0V
Receiver Input Threshold	+/-0.2	V	
Recv Input Threshold Hysteresis	50	mV	
(note 1)Logic Input Threshold Low	0.8 max	V	
(note 1)Logic Input Threshold High	2.4 min	V	
Receiver Logic Output High	3.7 min	V	VCC = 5V
Receiver Logic Output Low	0.1 max	V	I = 10uA
Receiver Input Resistance	500 min	Ohm	
Receiver Input CM Voltage	0-3	V	
Single ended output rise/fall time	15	ns	Rload = 54 Ohm, VCC=5.0V, Cload=100PF
Data Rate	200K	BPS	Rload = 500 Ohm, Cload = 500 PF to Ground on both outputs, VCC=5.0V

The Differential Receivers

The receivers for OCIA input signals are using either the voltage comparators or input buffers that thresholds at 2.5V with adequate hysteresis. The RS-485 receiver is shared among the RS-485 and the OCIA signals.

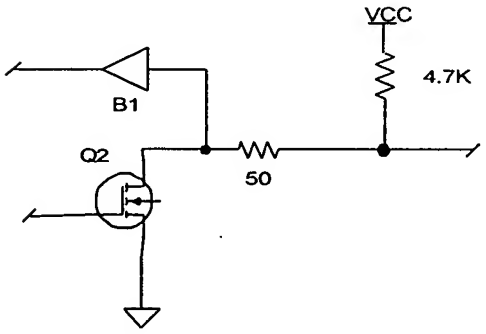
Electrical Specifications

Parameter	Typical	Unit	Condition
OCIA input voltage	0 - 5	V	
OCIA output low	0.6max	V	I = 5mA
OCIA output high	4.5 – 5.2	V	VCC = 5V
OCIA data rate	300Kmax	Hz	
Common mode voltage of receiver	3.5 max	V	
Receiver input Hysteresis	0.2	V	
(note 1)Propagation delay for both high-to-low and low-to-high	300max	ns	Input differential > 100mV

Note 1: parameters are specified for design simulation only. These parameters are not testable.

The Discrete Drivers and Receivers

The discrete drivers and receivers are provided for implementation of Synapse, Wand Emulation, Keyboard Wedges and OCIA interfaces. The circuit uses open-drain FETs to drive data in either direction. A current limiting arrangement should be provided if the enclosed driver cannot tolerate a direct short to 5V DC.



Electrical Specifications

Parameter	Typical	Unit	Condition
I/O PAD Voltage Range	+/-5V	V	Only for Q1 and Q2 and B1 and B2
B1 Logic Input Threshold Low	0.8 max	V	
B1 Logic Input Threshold High	2.4 min	V	
(note 1)Logic Output High	3.7 min	V	VCC = 5V
(note 1)Logic Output Low	0.1 max	V	I = 10uA
Driver Sink Current	5 min	mA	Vout = 0.6V
Driver Leakage Current	10 max	uA	Vout = 7V
Output short circuit current	220	mA	Vout = 7V
(note 1)Propagation delay on B1	40	ns	Cload = 50pF
(note 1)Turn-on Time of Q2	40	ns	
(note 1)Turn-off Time of Q2	40	ns	

Note 1: parameters are specified for design simulation only. These parameters are not testable.

The Analog Switches

The purpose of analog switches is to multiplex different interface signals in order to share the limited number of I/O pins. The implementation of any of the switches may not degrade or distort their associated signals (e.g. S6 or S14 may not clamp its signal to GND since the excursion of the signal is ±5V).

Electrical Specifications

Parameter	Typical	Unit	Condition
Logic Input Threshold Low	0.8 max	V	
Logic Input Threshold High	2.4 min	V	
Logic Output High	3.7 min	V	VCC = 5V
Logic Output Low	0.1 max	V	I = 10uA
Ron	35-160	Ohm	Vout = +5V or –5V
(note 1)Feed through Capacitance	0.5max	pF	
Switch Turn-on Time	30-200	ns	Rload = 1K, Cload = 50pF
Switch Turn-off Time	30-200	ns	Rload = 1K, Cload = 50pF

Note 1: parameters are specified for design simulation only. These parameters are not testable.

The switches S10-S13 are to demonstrate the output disconnection abilities of both RS-232 and RS-485 output. It does not dictate what the actual implementation will be. The actual design can probably be done with an output disable feature in the output drivers.

Status indicator LED driver

The micro controlled status indicator LED driver shall be able to sink at least 10mA of current to the GND reference continuously.

Power down and Wakeup Detector

There are three power-down controls governed by the 8051 process. They are the on/off f controls of the PLL oscillator, the –5V charge pump and the scanner power enable control. According to the USB 1.1 specification, a USB function allows a function device to draw less than 500uA of supply current during USB suspend, where as in the reset of interface modes, supply current of less than 1mA is generally desired. Therefore, in USB mode, the 8051 have to turn off both the PLL oscillator and the charge pump upon USB host suspension. Contrary, the charge pump will required to be on during RS-232 I/O mode. In order to meet this 1mA power requirement, both RS-232 output drivers need to be disabled during power down mode. That is done by the interface control decode to activate the RS_232_TXEN* signal to disable the RS-232 transmitters while the PLL is turned off. A power control override is provided to the external micro to disable the 8051 from controlling its power state.

The following on/off controls shall be provided for the power saving purposes:

- The –5V charge pump control (please refer to the interface control section for detail).
- The 1.84615MHz clock to the UART
  The 24MHz clock to the Micro
  The 48MHz clock to the USB SIE
- The power to the external (scanner) circuitry.

In order for the 8051 to control the power to the external micro and its own clock, two register each for both 8051 and external micro shall be provided. As is indicated, the 8051 can only read from the override register and the external micro can only read from the power state registers.

POWER CONTROL REGISTER (R/W) 8051 ADDR: 9420h

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R PWR	MIA PLL						

1: ON
0: OFF

Reset Default State is SCANNER PWR OFF and MIA PLL ON.

POWER OVERRIDE REGISTER (R) 8051 ADDR: 9421h

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R OVRIDE							

1: ON
0: OFF: Reset default

POWER STATE REGISTER (R) MIA ADDR: 0FH

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R PWR	MIA PLL						

1: ON
0: OFF

Reset Default State is SCANNER PWR OFF and MIA PLL ON.

POWER OVERRIDE REGISTER (R/W) MIA ADDR: 0EH

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R OVRIDE							

1: ON: override the power control
0: OFF: leave the power control via the 8051, which is the Reset default state

The detection of wakeup event will re-start the PLL oscillator from its off state and subsequently resume the 8051 processor. Events that can be used to generate the wakeup signal are the following:

- USB resume signal detected from sensing the falling edge on DIP input out of the transceiver.
- RS-232/485 Start bit detected (high to low transition out of the RS-232 transceiver)
- RS-232 handshake signal (CTS) switching from high to low out of the transceiver.
- Synapse Remote request (host pull the SYN_CLK signal)
- The external wakeup events, such as scan stand switch or trigger switch etc.
- OCIA Data detected from sensing the low to high transition on the OCIA_CLKOUT signal.

Provision shall be made to allow or disallow individual event from generating a wake up signal. Once the appropriate wakeup signal is detected, it will subsequently generate a wakeup output to be used by the external circuit such as the scanner micro.

WAKEUP MASK CONTROL REGISTER (R/W) ADDR: 940Eh

D7	D6	D5	D4	D3	D2	D1	D0
USB DIP	IBM 468X	OCIA CLKO	EXT WAKUP	SYN CLK		CTS	UART RXD

1: ENABLE
0: DISABLE : all 0 after external reset

WAKEUP STATUS REGISTER (R) ADDR: 940Fh

D7	D6	D5	D4	D3	D2	D1	D0
USB DIP	IBM 468X	OCIA CLKO	EXT. WAKUP	SYN CLK		CTS	UART RXD

1: ENABLE
0: DISABLE : all 0 after external reset

Download Detector

The download detector is an invert buffer that flows directly out to the external processor. Once the download enable is detected, the chip will retain the following states:

- 8051 will be put in its reset state.
- Interface selection will be overrides to RS-232.
- The Charge Pump will remain on regardless.
- The Scanner power control will be enabled at all time.
- The RS-232 TXD and RXD signals are by-passed to the external processor.

3.3V Regulator

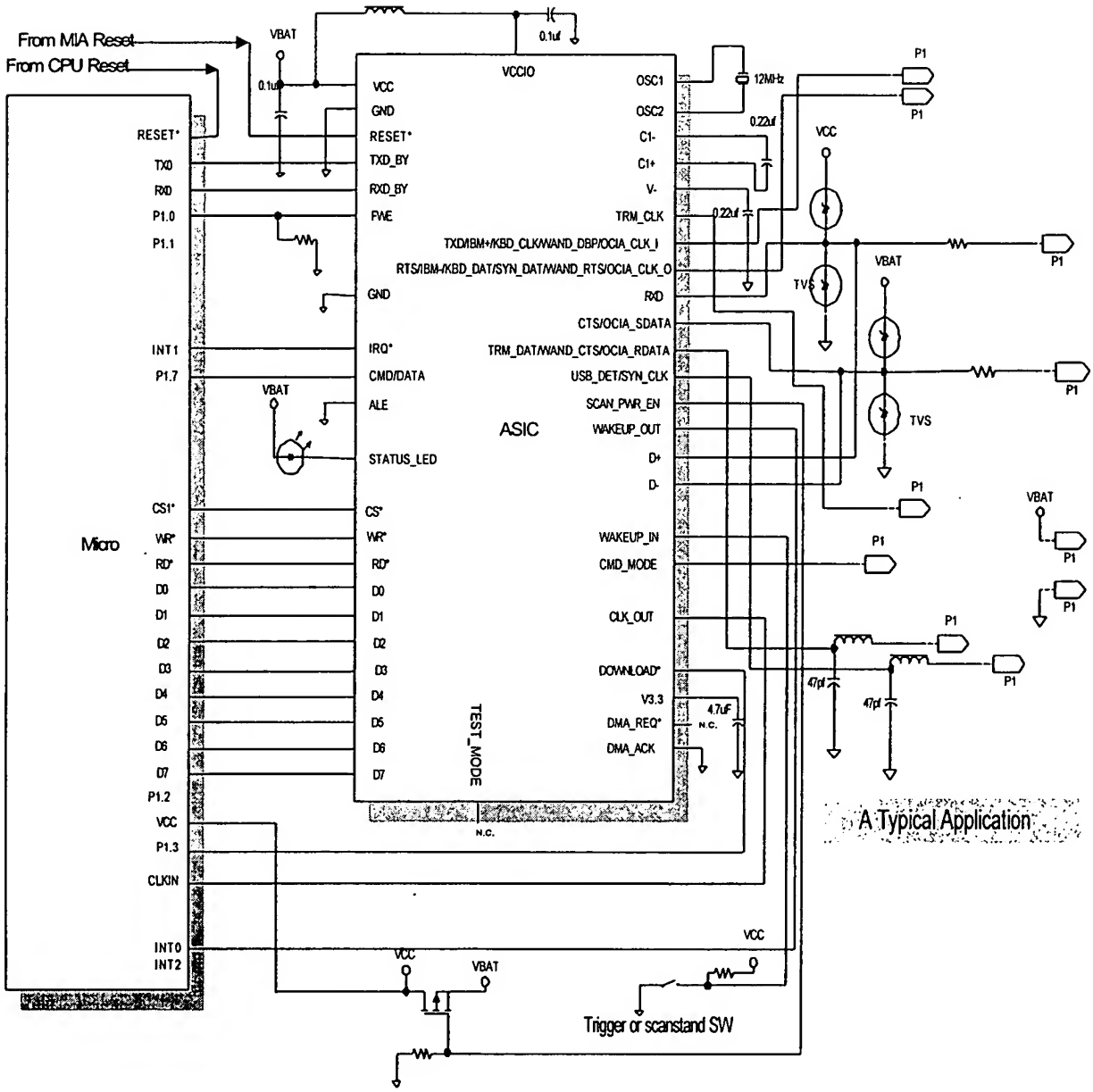
The 3.3V Regulator output is used to power the USB core and USB transceiver. A 4.7uF low-ESR tantalum capacitor shall be used to stabilize the voltage regulator.

Development Tools

At least the following development tools shall be made available prior to the beginning of the ASIC development. Development board (evaluation prototype) can be a plus to shorten the development time but it is not mandated.

- The development suite (C compiler, Assembler, Linker are musts, but the simulator is optional)
- The In-Circuit Emulator for the micro. A special bond-out chip with additional I/O pins for ICE is a must for software development.

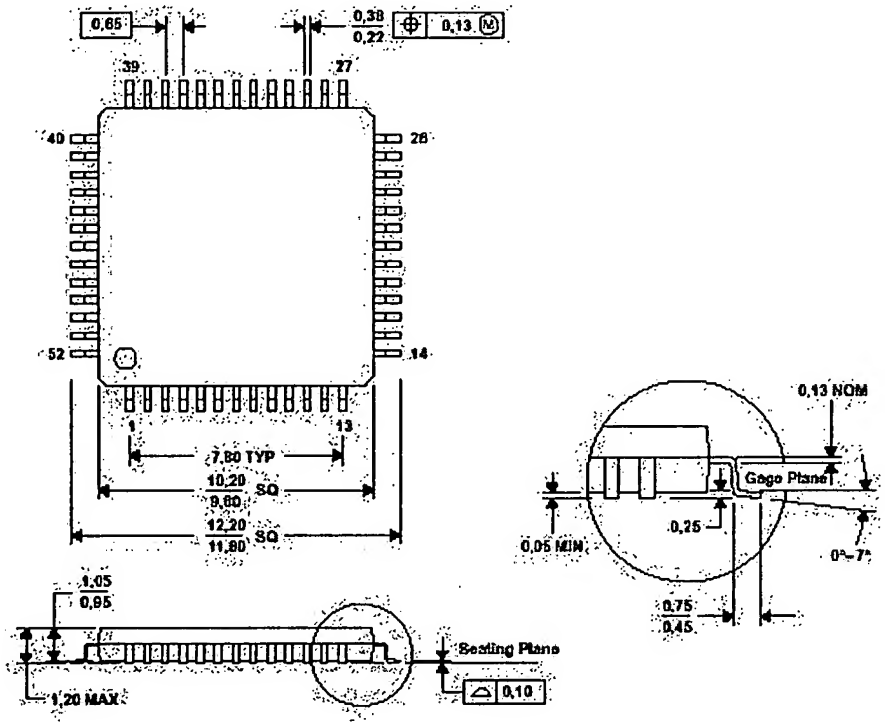
A typical application of this ASIC is illustrated in the following diagram.



A Typical Application

Package

The standard chip should be packaged in the smallest package possible, considering both thermal dissipation and cost impact. The preferred packages are TQFP52.



As for the special bound-out chip, a 120-pin PGA ceramic package will be used.

Marking

TBD

Temperature Range

Operating: -40 to 85°C
Storage: -65 to 120°C

Compliance

Considering the regulatory requirements for those applications that this device will be integrate in, the device will be subjected to the following tests. Hence, the design of this device shall pass these test requirements.

ESD

±8KV on the following dedicated I/O signals.

1. TXD/IBM+/KBD_CLK/WAND_DBP/OCIA_CLK_I
2. RTS/IBM-/KBD_DAT/SYN_DAT/WAND_RTS/OCIA_CLK_O
3. RXD
4. CTS/OCIA_SDATA

Measure the radiated field from the unit over the frequency range 30MHz to 1GHz, as per C.I.S.P.R. Class B test conditions.

Radiated and Conducted EMI Susceptibility: Expose the unit to 10 V/m over the frequency ranges 10kHz to 1GHz.

Electro-Fast Transients (EFT Burst): Subject cable to ±1kV amplitude and 5kHz high current interference.

Transient Susceptibility: Inject 150ns and 50us transient on the DC lines.

Aeroflex UTMC Proprietary

Subject: Symbol MIASIC IDR Minutes and Actions
Date: April 12, 2001

Agenda:

- Introductions
- Schedule Milestones
- Specification Issues and Questions
- Analog I/O Simulation Review.
- Oscillator and PLL data Review.
- Questions and Action Items
- Wrap-up

1. **Introductions; general comments.**

   Attendees: Symbol: Peter Musteric and Tony Chang. UTMC: Tom Richardson, Ben Valdez, David Kerwin (by teleconference). For specific topics: Tom Sutton, Nevenka Cuk, Quyen Ton.

   Hyundai has spun off Hyundai Electronics America (as of 4/9/01) as Hynix Semiconductor.

   David believes that distancing Hynix Semiconductor from rest of Hyundai should have a positive effect, since other parts of Hyundai are currently losing money and Hynix Semiconductor is financially healthy.

2. **Schedule Milestones.**

   Symbol expressed time-to-market concerns. Would like to see schedule pulled in at least 3 weeks. Two weeks of fab expedite may be possible by paying a $15K expedite fee (refundable if they Hynix doesn't meet the expedite). Some expedite (2-3 days) will be possible from ASAT (packaging).

   If there are no more specification changes, delays from digital design, or unforeseen technical problems, UTMC will make every attempt to pull in the design schedule by at least a few days.

❖ **Action**: Symbol (Peter) to add line item to Purchase Order to expedite fab.

Discussion about number of packaged prototypes are needed in the initial build. UTMC preference is 2500. (If more prototypes are required, 5K could be packaged initially.) Second delivery could be 15.5K in about 3 weeks time.

❖ **Action**: Symbol (Peter) will verify if 2500 packages prototypes will be adequate for their needs.

3. **Specification discussion.**

   - I/O name changes:

     SCANSTAND changed to SCAN_PWR_EN (? Check this on spec)

     SCAN_STAND → WAKEUP_IN

     WAKEUP → WAKEUP_OUT

     A0 → CMD/DATA

Aeroflex UTMC Proprietary

- Reviewed *preliminary* floorplan & pad locations (product and ICE versions).
- Power budget. Power estimate has changed due to change in size of pumper capacitor from 0.1 uF to 0.2 uF. (Reason: RS232 Driver Test xx) Current estimate of pumper current is 1.3 mA.

❖ **Actions**: Symbol (Tony) will decide whether to increase the 1 mA Power Down specification. UTMC will run additional simulations if Symbol can not accomodate this.

- Page 16 of spec. Need to add Pull-up and Pull-down currents to Digital I/O specification.
- Page 39 of spec. Change "No more than 120 KBPS" to "Maximum of 120 KBPS"
- Page 41 of spec. Discrete Driver Section: Change Vout to 5V.
- Need to add fault coverage to spec.
- Page 16 of spec. 3V digital I/O. Need to specify Bidirectional I/O rise/fall time. Is 4–20 nS a final goal, or can it be faster? Tony said that the 3V Bidir should meet the current specs listed for the digital IO. Simulations were run and show that R/F fall between these bounds at 3V, but not at 5V (fast process,

❖ **Actions**: Symbol (Tony) will address these (5) specification issues.

4. Analog I/O Simulation Review.

Schematic and simulation results reviewed for:

- RS232 Receiver. Hysteresis is 200 mv in Spec. Simulations are showing 200 mV worst case. Symbol says this should be interpreted as typical.

❖ **Actions**: UTMC (Tom R.) will modify design to give 200 mV typical.

- **RS232 Driver**. No issues.
- **RS232 Driver Test**. No issues.

  Note: Tom R. suggests that Symbol might wish to review preferred value of pumper capacitor (0.1 uF, 0.2 uF). Trade-off between maximum power-down current vs. max value of –5V (i.e., min absolute value).

❖ **Actions**: Tom R. will simulate power with 0.1 uF.

- **Negative Pumper**. No issues.
- **RC Oscillator**. No issues.
- **Discrete Output**. No issues.
- **Discrete Bidirectional**. No issues.
- **–5V Discrete Bidirectional**. No issues.
- **USB Transceiver**.

  Note: TR/TF matching simulations slightly out of spec (–11.5% vs. – 10% spec) under the condition: (T <–30° C, slow process, low 3.3V supply & large feedback capacitor.)

❖ **Action**: Symbol to decide whether to sign-off on this spec item.

Note: USB recommends but does not specify differential hysteresis. UTMC USB transceiver has 150 ± 50 mV hysteresis. Symbol will research typical hysteresis values of USB products.

❖ **Action**: UTMC (Tom S.) to add pull-up to USB D+ and pull-down to USB D–.

- **RS485 Driver.**

  Note: Rise time simulation slightly out of spec at –40° C.

❖ **Action**: Symbol to decide whether to sign-off on this spec item.

- **RS485 Receiver.**

❖ **Action**: UTMC (Tom R.) to change the OCIA inputs to add pull-up & pull-down.

5. **Oscillator and PLL data Review.**

   Note: The effort to characterize Symbol's candidate crystals and resonators is in progress.

   Test results to date: The ceramic resonators we have been testing do not always start oscillations reliably; the crystals do start reliably. Resonator startup times are faster (few µS vs. few mS) and resonator draws twice the current.

   Plan: UTMC will retain the existing oscillator circuit and will test the circuit with different resonators (supplied by Symbol) if Symbol wishes.

❖ **Action**: UTMC will investigate whether some packaged YX01's can be provided to Symbol for crystal & resonator experiments.

6. **Digital Netlist**

   Tony and Quyen ran (pre-route) timing simulations with Symbol's testbench and digital netlist. Seeing same errors as before. Quyen has sent copy of error messages to John.

   Note: Quyen will continue simulating the netlist with remaining testbenches and review results with Symbol and UTMC design team.

7. **Questions and Action Items**
8. **Wrap-up**

EXHIBIT G

Multi-Interface ASIC (MIA) Overview

Peter Musteric

March 19, 2001

Symbol Technologies
Confidential

MIA Overview

- MIA Developers
- Why MIA?
- Goals of Implementation
- MIA Technical Challenges
- System Overview, Operation and Implications
- Schedule
- MIA is not ...
- Operations Issues
- Program Issues
- Summary

MIA Developers

- Tony Chang
- John Fioriglio
- Rizwan Alladin
- Brad Morris
- Rob Lieb
- Others to be added shortly....

Why MIA?

- Channel Partners, Operations, and Engineering desire to minimize configurations.
- Marketing desire to support Multi-Interface capability at a low cost point.
- Competitors offered channel friendly multi-interface solutions

Why MIA?

- Current Multi-Interface Solutions
  - Example using the LS 400Xi
    - LS4004i --- RS232, Synapse
    - LS4005i --- IBM4683, Synapse
    - LS4006i --- Keyboard Wedge, Synapse
      - *Total of three configurations*
  - LS4005i, LS4006i, M2005, M2007 and LS6005 all use the Synapse uP to integrate respective interface
    - Additional Cost ~$3.00
  - Synapse Model – Additional cost > $20

MIA Goals

- Cost Effective Solution – Target Cost $3.25
- Leverage Previous Interface Work
  - The "Synapse Benefit"
- Support Most Popular Interfaces
  - RS 232
  - P/S 2 Kybd
  - USB
  - IBM 46XX
  - Wand
  - Synapse

MIA Goals (cont.)

- Provide flexibility supporting multiple interface variants (e.g.int'l kybds)
- Work with multiple decoder architectures
- Minimize development costs both capital costs and recurring Engineering development efforts
- Provide clean partition between interface and decoder S/W

MIA Technical Challenges

- Development of Mixed Mode ASIC
- Embedded Core w/Flash
- Development Environment
  - How does an ICE work with this device
- Use existing Universal Cables
- Ensure no damage for "incorrect installations"

MIA System Overview

- Embedded DW51 Core
  - 8031 uP derivative used in IMP
  - Similar architecture to Synapse uP
- 32K embedded Flash
- 2K RAM
- USB Interface controller
- Analog/Digital Interface Circuitry

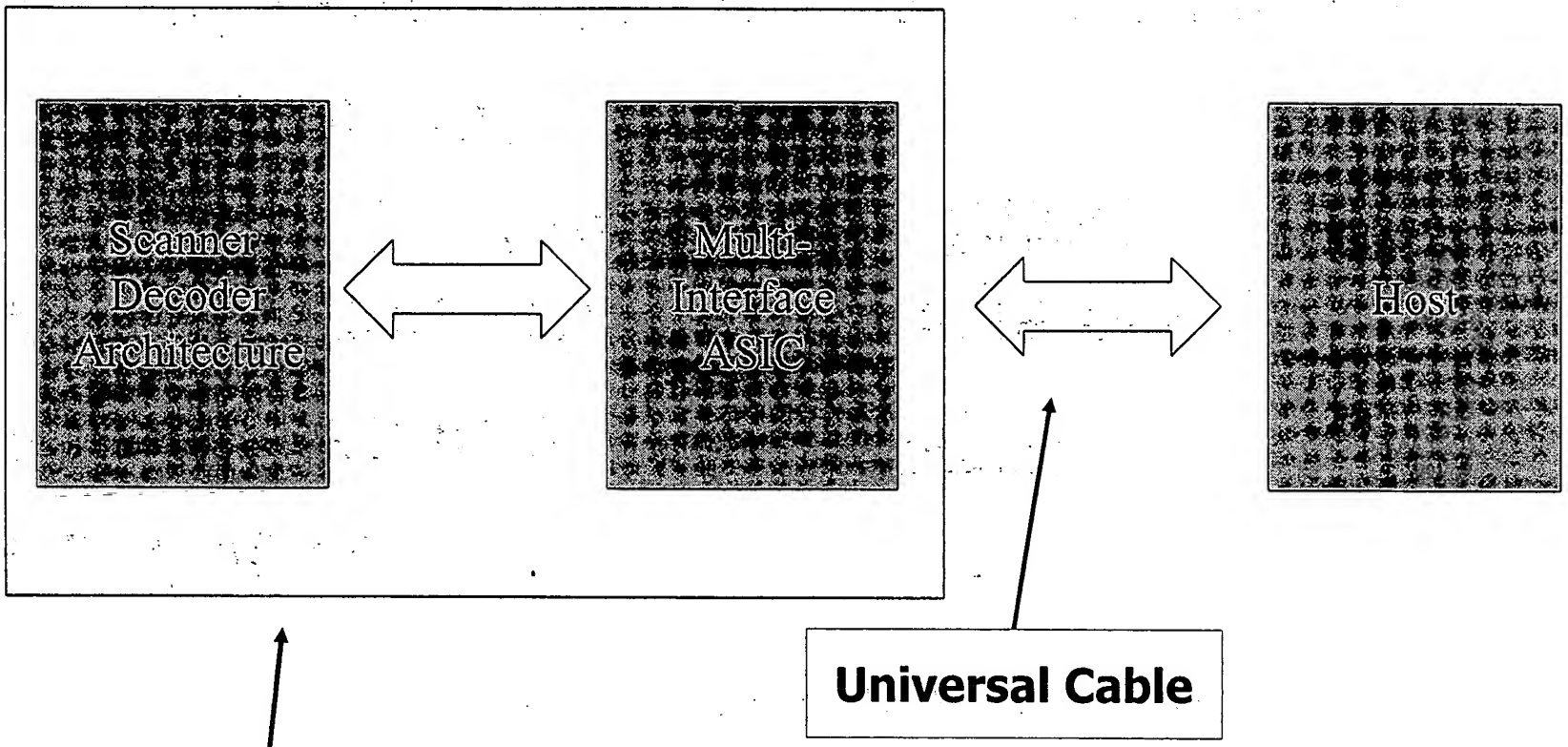
MIA Features

- Supported Interfaces
  - RS232 (EIA levels, +/- 5 volts, 115 Kbaud)
  - USB (Bulk, Interrupt and Isochronous)
    - HID Keyboard Emulation
    - IBM Yellowstone
    - Symbol's Proprietary Implementation (Keystone)
  - PS/2 Keyboard Emulation
  - Wand Emulation
  - RS485
  - Synapse
  - Flash Download Capability

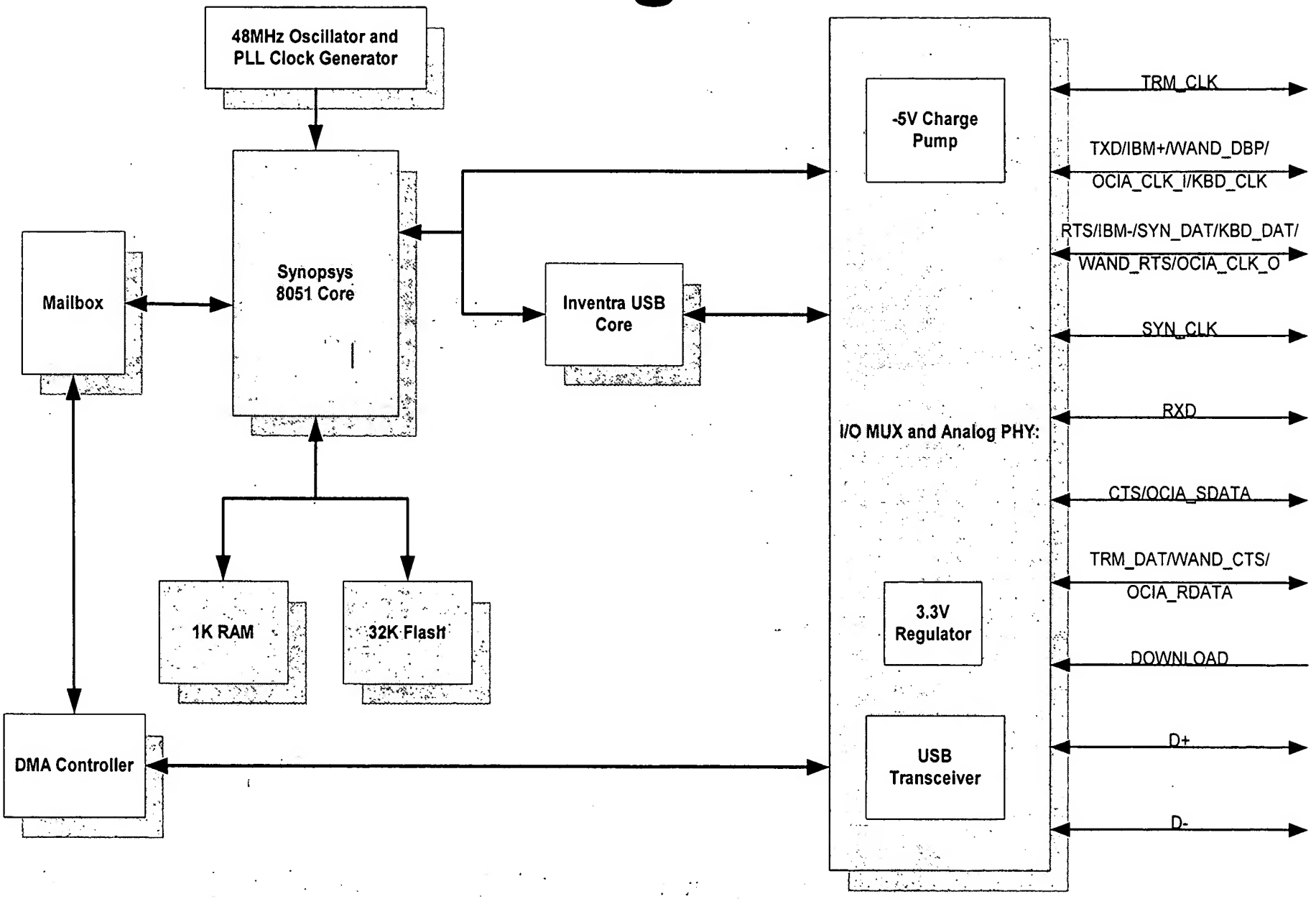
MIA Features

- 5 Volt Vcc
- Packaged in a 52 pin TPQFP
- Mixed Mode (RS232 charge pump, USB engine, 3.3V Regulator, Interface Multiplexing)
- ASIC expected to be used in multiple scanner programs

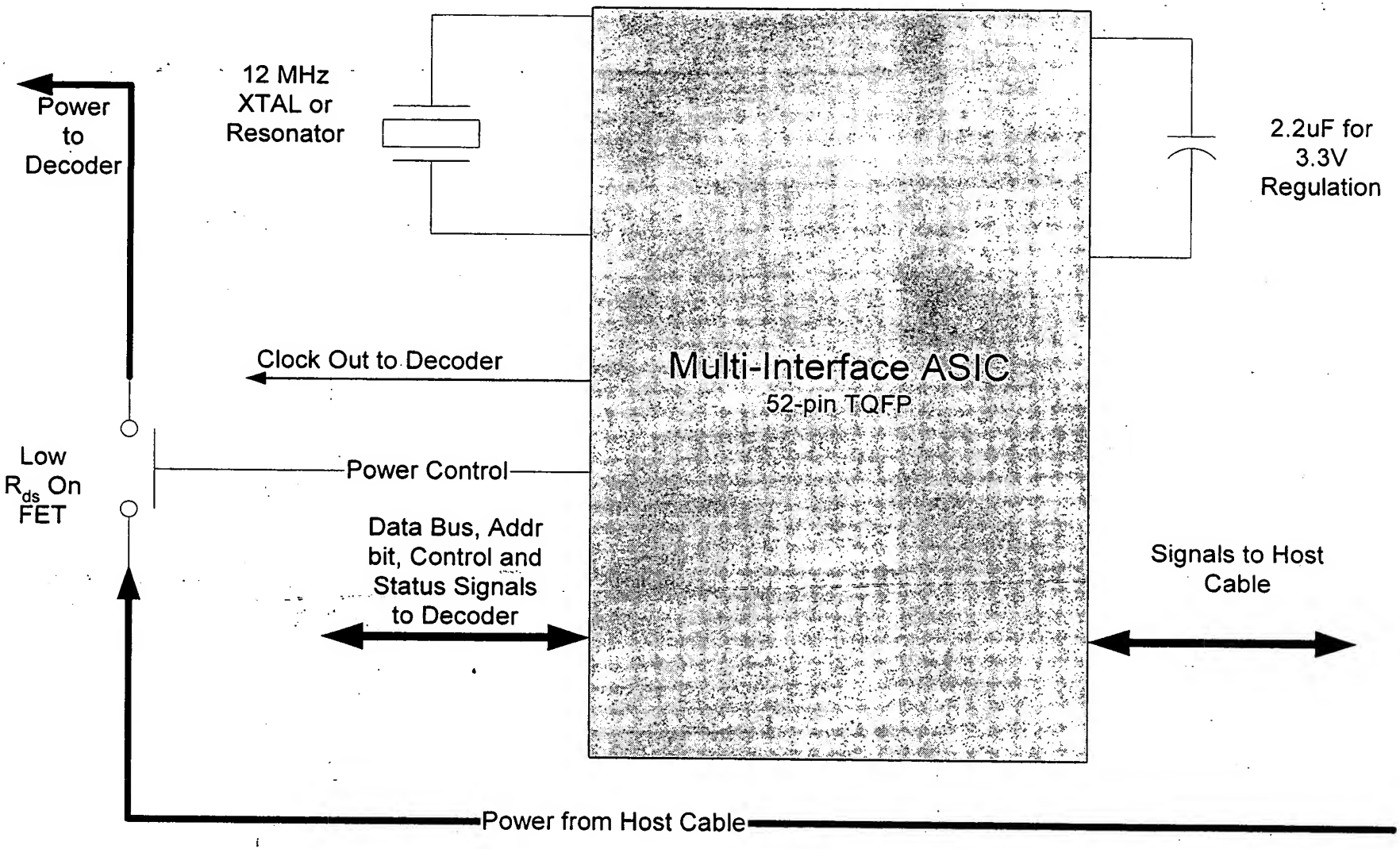
Scanner with MIA Overview



MIA Block Diagram



What external circuitry does MIA need?



Integration Implications

- Software
  - Significant effort to port interfaces to MIA environment.
  - Scan/decode and interface software will have to co-exist on same core
  - Current Flash Download utility will have to be enhanced
  - Significant effort to re-validate Interface code.

Integration Implications

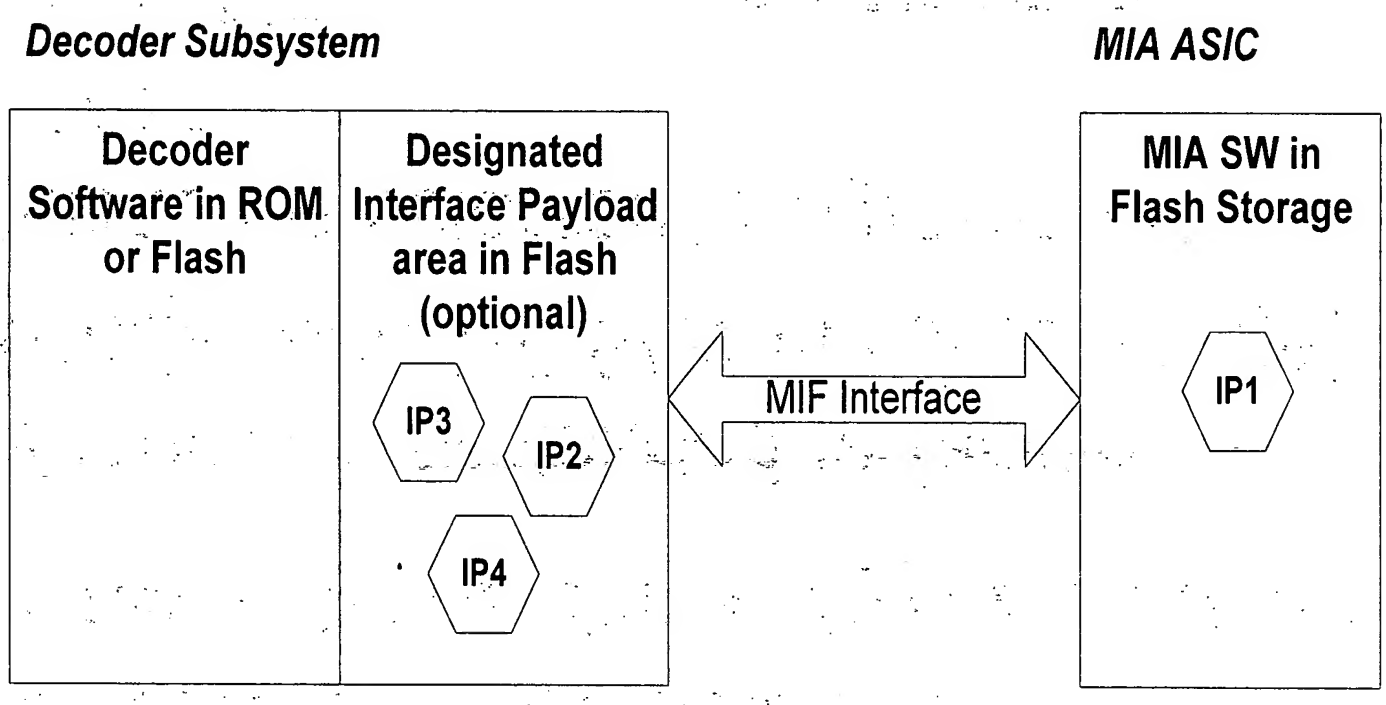
- Hardware
  - Future platforms will need necessary code space to support all the interface combinations.
  - More port pins needed to interface to proposed ASIC. (Worse Case = 8)
  - USB implementation may still require external logic to meet stringent current draw requirements.

MIA Initial Operation

"Taking a book from the Library"

- Scanner is downloaded in factory (Decoder and I/F S/W in same image)
- Interface is selected/programmed in scanner
- Correct I/F image is downloaded to MIA flash

MIA Interface Payload



Flash Downloading w/ MIA

- Flash download is transparent to MIA
- Unique download cable attached
- MIA Processor held in reset
- Hex Image is loaded to decoder Flash

Interface Switching – 3 Conditions

- I/F code not available in Scanner or MIA
  - User is given error beeps
  - Needs to install intended I/F code from ...
- I/F code available in MIA*
  - Decoder sends "Reset Request"
  - MIA activity suspended
  - Decoder updates MIA settings

Interface Switching (cont'd.)

- I/F code available in Scanner* (I/F Payload Area)
  - Decoder sends "Reset Request"
  - MIA activity suspended
  - Decoder updates MIA Flash image
  - Decoder updates MIA settings

Interface Switching

- Changing I/F will not damage electronics, but may cause gibberish on signal lines to host
- Suggested behavior for changing host types (e.g. RS-232 to USB)
  - System install temporary null host
  - On power up (after cable change), new host is installed
- Comments????? (especially you Marketing folks!)

Scanner w/MIA : Normal Operation

- Scanner decodes barcode
- ADF (if enabled) is performed
- Decoder transfers data to MIA via mailbox (MIF)
- MIA formats data and sends to the host

Actually, this is a lot like Synapse and the SDCI protocol!

MIA Development Environment

- Currently developing FPGA development system
- Creating Bond out version of the device
  - All uP pins are external
  - 1 in 6 die/wafer
  - Packaged in 120 PGA package

MIA Utilities

- Programming capabilities
- Adding new / alternate Interface code (Interface Payload Configuration Utility)
- Parameter selection and storage

Schedule Milestones

Program Milestones	Plan	Comments
Design Kickoff	12/2	
Preliminary Design Review	12/13	
Symbol Net list to UTMC	3/9	
S/W Design Doc/Rev	3/23	S/W Dates are preliminary and looking to improve them
S/W Coding/ and unit test	7/20	Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	4/30	
ASIC Proto Fab (start)	5/8	Will need to order qty to cover Alpha/pilot builds
Protos Received	7/15	May be able to improve date with $'s, ICE version earlier
H/W S/W Integration & Testing	8/2	
S/W Validation	8/30	
Proto Acceptance	8/15	
Major Mfg. Milestones		
Risk Production availablity	8/15	Protos available prior
Qual Completion	TBD	Final Product dependent
Rev A Release	8/31	Component Level & S/W

What Not to Expect

- Interfaces not supported: Legacy Systems, OCIA (actually H/W is in ASIC)
- Cost burdens less expensive interfaces.
  - Example:
    - Keyboard Wedge-only solution = ~$0.50
    - Keyboard Wedge solution via ASIC > $3.00
  - The single dedicated interface is always the lowest cost solution

What Not to Expect (cont'd.)

- May not be viable solution for all scanner products
  - Costly for low-end consumer products
  - Will not support USB 2.0 high speed data transfer rates (up to 480 Mbits/second)

Operations Issues

- Unique ID for USB programmed at Manufacture (similar to RL 474/5)
- Capability to program/select interface at time of packaging
- Default MIA payload – what will it be?
- Appropriate testing – not all possible interfaces, but an intelligent subset

Program Issues

- Schedule is very tight for all PSC variants – first silicon success required
- Power Scan variant poses potential issues with use of existing PSC cables
- All products should have PCB waiting to drop in MIA prototypes
- Need forecast for Alpha qty's and Q4 usage !!!

Additional MIA Reading is available in the following documents:

- Symbol's SMI (Scanner MIA Interface) Interface (Rev. 0.9)
- Symbol's MIF (Mailbox Interface) Interface (Rev. 0.9)
- Multi-Interface ASIC Specification (Rev. 5)

MIA Summary

- A significant effort for both H/W and S/W
- A flexible, cost effective solution for multi-interface applications
- A re-usable design to be deployed in future scanners as easily as Synapse

MIA Overview – The End!

⌘Questions ?

Scanner Program Summary

EXHIBIT H

Report Date: 3/15/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Rob Lieb, Brad Morris

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

Program Milestones	Original Plan	Actual	Comments
List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23		(S/W Dates are preliminary)
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	Late April	
ASIC Proto Fab (start)	4/13		Will need to order qty to cover Alpha/pilot builds
Protos Received	6/22		Date may slip to mid-July
H/W S/W Integration &	8/2		(S/W Dates are preliminary)

Testing			
S/W Validation	8/30		(S/W Dates are preliminary)
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availablity	7/15		
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- 5 Volt tolerant USB driver proving to be a challenge – may impact schedule additional week
- Senior Designer at UTMC had death in family – UTMC has indicated that schedule will take a two to three week delay and will not be ready for final net list until 3/9 - currently working to minimize overall impact with UTMC
- Will need to provide PSC development platform and supporting documentation including H/W spec, System Design Spec (in development). Working with Paul Waxelbaum to coordinate and schedule activities
- Reviewing interface pin-outs for potential damage in incorrect host/ incorrect cable combination is used.
- Schedule is based on one turn of ASIC

Design Update:

- Preliminary netlist delivered to UTMC on 3/9/01
- Completed review of pin-outs – will have to add diode to Keyboard wedge cable to maintain Universal cable pin out
- BOM status in SAP : N/A

Material Status:

- Risk production will have to be ordered at prototype time to support other program pilot builds.

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Fixture requests submitted?
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues

NPDC PCB Plan Dates:

- N/A – handled at product level

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 7/3/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

Program Milestones	Original Plan	Actual	Comments
List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/3 ~~7/29~~	Late July date includes 2 week expedite fee of $15K (BGA

			ICE parts)
H/W S/W Integration & Testing	8/2	8/6	
S/W Validation	8/30	8/31	
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availability	8/5	8/10	Protos packaged in final package (52 pin PTQFP)
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- 2K plastic parts available in August – Additional 15K parts can be packaged w/ 3week turn-around
- Schedule is based on one turn of ASIC

Design Update:

- Device is now in fabrication at Hynex – wafers due out 7/27.
- Metal change required due to logic sense of USB Suspend signal inverted. Discovered in FPGA proto hours before full reticule set was created. Schedule impact – 3 days
- Design Database (netlist) transferred to Hynex on 5/29 for fabrication of protos.
- Ran into Scan Test Chain timing issue. Will be addressed in future spin if necessary (on UTMC's nickel) – does not, I repeat, not impact functional performance.
- CDR completed on 5/17 at Aeroflex/UTMC's West Coast Design Center
- FPGA prototypes functional and being used for code development; Synapse, IBM, RS-232 are well along. H/W verified for Wand and Keyboard wedge, still testing/developing USB.
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)
- BOM status in SAP: N/A

Material Status:

- Placed $10K Engineering fee for metal mask changes due to USB Suspend signal inversion.
- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.

- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:
- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:
- PCBs should be available to run in early August for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:
- N/A – Handled at product level

Packaging:
-

Qual:
- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 7/18/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

Program Milestones	Original Plan	Actual	Comments
List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/3 ~~7/29~~	Late July date includes 2 week expedite fee of $15K (BGA

			ICE parts)
H/W S/W Integration & Testing	8/2	8/6	
S/W Validation	8/30	9/17	
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availability	8/5	8/10	Protos packaged in final package (52 pin PTQFP)
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- 2K plastic parts available in August – Additional 15K parts can be packaged w/ 3week turn-around
- Schedule is based on one turn of ASIC

Design Update:

- Device is now in fabrication at Hynex – wafers due out 7/27.
- Metal change required due to logic sense of USB Suspend signal inverted. Discovered in FPGA proto hours before full reticule set was created. Schedule impact – 3 days
- Design Database (netlist) transferred to Hynex on 5/29 for fabrication of protos.
- Ran into Scan Test Chain timing issue. Will be addressed in future spin if necessary (on UTMC's nickel) – does not, I repeat, not impact functional performance.
- CDR completed on 5/17 at Aeroflex/UTMC's West Coast Design Center
- FPGA prototypes functional and being used for code development; Synapse, IBM, RS-232 are well along. H/W verified for Wand and Keyboard wedge, still testing/developing USB.
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)
- BOM status in SAP: N/A

Material Status:

- Placed $10K Engineering fee for metal mask changes due to USB Suspend signal inversion.
- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.

- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:
- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:
- PCBs should be available to run in early August for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:
- N/A – Handled at product level

Packaging:
-

Qual:
- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 8/15/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

Program Milestones	Original Plan	Actual	Comments
List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/9 ~~7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		8/28	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	9/28	
Proto Acceptance	7/20	9/15	
Major Mfg. Milestones			
Risk Production availability	8/5	9/4 (8/28)	Protos packaged in final package (52 pin PTQFP) – (possible if wafers are shipped direct to packaging fw/o test and drop shipped to Omni in Singapore).
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	9/28	Component Level & S/W
Initial production Start	7/20	9/15	Eight week lead time for production parts

Critical Programmatic Issues:

- UTMC discovered a problem in the Flash cell. Currently working on a metal fix. Will delay availability of plastic parts until approx. September 4th (can be improved to 8/28)
- Flash delay will impact final S/W integration testing
- 6K plastic parts available in September – Additional 10K parts can be packaged w/ 3week turn-around
- Schedule is based on one turn of ASIC

Design Update:

- Received ICE prototypes on 8/9
- All interfaces have been tested and appear functional, Decoder/MIA interface (MIF) is functional. Can program and read the Flash on chip (unfortunately only 64 bytes/sector). There is an issue with the Oscillator and the switching in the Keyboard Wedge pull-ups – both of these changes are addressed in the metal change for the Flash and will be incorporated in the Flash block metal changes.
- Rev 2 Prototypes (metal change for Flash etc.) are entering metal today.
- Metal change required due to logic sense of USB Suspend signal inverted. Discovered in FPGA proto hours before full reticule set was created. Schedule impact – 3 days
- Ran into Scan Test Chain timing issue. Will be addressed in future spin if necessary (on UTMC's nickel) – does not, I repeat, not impact functional performance.
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)

Material Status:

- Placed PO for Risk production 6Kparts for September, October, and November
- Placed Letter of Subcontract to allow AeroFlex/UTMC
- Placed $10K Engineering fee for metal mask changes due to USB Suspend signal inversion.
- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early September for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 8/29/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

Program Milestones	Original Plan	Actual	Comments
List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/9 ~~7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		9/1 ~~8/28~~	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	9/28	
Proto Acceptance	7/20	9/15	
Major Mfg. Milestones			
Risk Production availability	8/5	9/4 (8/30)	Protos packaged in final package (52 pin PTQFP) – (possible if wafers are shipped direct to packaging fw/o test and drop shipped to Omni in Singapore).
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	9/28	Component Level & S/W
Initial production Start	7/20	9/15	Eight week lead time for production parts

Critical Programmatic Issues:

- Corrected ASICs are out of FAB – currently in packaging. 400 PQFP parts due on Friday. ICE Parts have been delayed due to aircraft issues, are now expected this Saturday.
- Additional parts will be packaged and shipped direct to Omni for Smart Line alpha as soon as we give the approval.
- USB OHCI interface not performing consistently; all other interfaces appear to be working.
- Schedule is based on one turn of ASIC

Design Update:

- Rev. 2 Protos expected this week with corrected Flash, Oscillator, and Interface enable circuitry.
- Received ICE prototypes on 8/9
- All interfaces have been tested and appear functional, Decoder/MIA interface (MIF) is functional. Can program and read the Flash on chip (unfortunately only 64 bytes/sector). There is an issue with the Oscillator and the switching in the Keyboard Wedge pull-ups – both of these changes are addressed in the metal change for the Flash and will be incorporated in the Flash block metal changes.
- Rev 2 Prototypes (metal change for Flash etc.) are entering metal today.
- Metal change required due to logic sense of USB Suspend signal inverted. Discovered in FPGA proto hours before full reticule set was created. Schedule impact – 3 days
- Ran into Scan Test Chain timing issue. Will be addressed in future spin if necessary (on UTMC's nickel) – does not, I repeat, not impact functional performance.
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)

Material Status:

- Placed PO for Risk production 6Kparts for September, October, and November
- Placed Letter of Subcontract to allow AeroFlex/UTMC
- Placed $10K Engineering fee for metal mask changes due to USB Suspend signal inversion.
- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early September for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 9/12/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30~~-5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/9~~-7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		9/1 ~~8/28~~	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	9/28	
Proto Acceptance	7/20	9/15	
Major Mfg. Milestones			
Risk Production availability	8/5	9/4 (8/30)	Protos packaged in final package (52 pin PTQFP) – (possible if wafers are shipped direct to packaging fw/o test and drop shipped to Omni in Singapore).
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	9/28	Component Level & S/W
Initial production Start	7/20	9/15	Eight week lead time for production parts

Critical Programmatic Issues:

- Received untested "corrected FLASH" devices on 9/1 and 9/4 (plastic parts, PGA).
- Plastic parts had 13x13 mm packages instead of the 10 x 10 mm package body. New 10x10 packaged parts are being shipped to Symbol
- Functionality has been verified, but yields are very low (<50%). This is, in part, due to that fact that devices were not tested and adjusted (Band Gap reference) prior to shipment.
- Experiencing an "over erase" condition that causes good Flash to appear bad, can be recovered by extra steps to write "1's" to device
- Working with UTMC to complete test fixture and screening procedure

Design Update:

- Have verified functionality of each major design block
- Part numbers assigned: 51-13130-057 (Production part), 51-13130-058 (I.C.E. part)

Material Status:

- Have held the assembly of 9K risk units pending results of current evaluation – will need parts for Olympus Smartline Qual build. Want units to be screened.
- Placed PO for Risk production 6Kparts for September, October, and November
- Placed Letter of Subcontract to allow AeroFlex/UTMC
- Placed $10K Engineering fee for metal mask changes due to USB Suspend signal inversion.
- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early September for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 9/26/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/9 ~~7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		9/1 ~~8/28~~	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	9/28	
Proto Acceptance	7/20	9/15	
Major Mfg. Milestones			
Risk Production availability	8/5	9/4 (8/30)	Protos packaged in final package (52 pin PTQFP) – (possible if wafers are shipped direct to packaging fw/o test and drop shipped to Omni in Singapore).
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	9/28	Component Level & S/W
Initial production Start	7/20	9/15	Eight week lead time for production parts

Critical Programmatic Issues:

- Struggling with "good part" availability for S/W development
- Chasing USB issue – very poor yields
- Working with UTMC to improve their screening capability
- Received 400 "slow process" (more reliable Flash operation) parts 9/20 – unable to evaluate plastic parts due to fixture issues
- Material is staged at metal should a change be required – these parts would be available in three weeks once change was completed. If silicon change is required, the lead time would be approximately 12 weeks.
- Functionality has been verified on ICE devices, but yields are very low (<50%).
- Experiencing an "over erase" condition that causes good Flash to appear bad, can be recovered by extra steps to write "1's" to device

Design Update:

-
- Have verified functionality of each major design block
- Part numbers assigned: 51-13130-057 (Production part), 51-13130-058 (I.C.E. part)

Material Status:

- Approx. 10 additional "Slow process" ICE devices are being fabricated
- 220 Slow process packaged (10x10 PQFP) parts are in our lab
- 180 Slow process parts are at UTMC waiting for improved test screening
- An additional
- Have held the assembly of 9K risk units pending results of current evaluation – will need parts for Olympus Smartline Qual build. Want units to be screened.
- Placed PO for Risk production 6Kparts for September, October, and November
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early September for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date:10 /10/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	~~8/9~~ ~~7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		9/1 ~~8/28~~	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	9/28	
USB Issue Resolution			
USB Trouble shooting	10/19	10/19	
USB "Fix"	10/26	10/26	
USB Parts	11/15	11/15	Assuming metal fix
Proto Acceptance	7/20	11/29	
Major Mfg. Milestones			
Risk Production availability	8/5	10/29 (8/30)	Protos packaged in final package (52 pin PTQFP) – (possible if wafers are shipped direct to packaging fw/o test and drop shipped to Omni in Singapore).
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	11/30	Component Level & S/W
Initial production Start	7/20	9/15	Eight week lead time for production parts

Critical Programmatic Issues:

- Continuing to trouble shoot USB issue – "see the problem" Not responding to to "IN Packet", looking for root cause
  - UTMC on site next week with equipment
  - FIB'd production parts (samples) this week
  - Additional ICE Parts due 10/12
- Additional material, 25 wafers, has been started and will be staged prior to metal – this will allow any metal fix to be approximately 2 weeks away from a metal change fix.

Design Update:

- Evaluating the contingency of placing USB Synapse on Smart Line & NG Hot Shot
- Have verified functionality of each major design block
- Part numbers assigned: 51-13130-057 (Production part), 51-13130-058 (I.C.E. part)

Material Status:

- Six hundred production parts will be available week of 10/29
- Have held the assembly of 9K risk units pending results of current evaluation – will need parts for Olympus Smartline Qual build. Want units to be screened.
- Placed PO for Risk production 6Kparts for September, October, and November
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early September for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 8/1/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

Program Milestones	Original Plan	Actual	Comments
List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/9 ~~7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		8/28	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	9/28	
Proto Acceptance	7/20	9/15	
Major Mfg. Milestones			
Risk Production availability	8/5	9/4	Protos packaged in final package (52 pin PTQFP)
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- UTMC discovered a problem in the Flash cell. Currently working on a metal fix. Will delay availability of plastic parts until approx. September 4th.
- Flash delay will impact final S/W integration testing
- 6K plastic parts available in September – Additional 10K parts can be packaged w/ 3week turn-around
- Schedule is based on one turn of ASIC

Design Update:

- Initial Flash block design requires metal change – in process. May address Scan Chain issue at the same time.
- Initial silicon out of fab – now being packaged in PGA packages.
- Metal change required due to logic sense of USB Suspend signal inverted. Discovered in FPGA proto hours before full reticule set was created. Schedule impact – 3 days
- Design Database (netlist) transferred to Hynex on 5/29 for fabrication of protos.
- Ran into Scan Test Chain timing issue. Will be addressed in future spin if necessary (on UTMC's nickel) – does not, I repeat, not impact functional performance.
- CDR completed on 5/17 at Aeroflex/UTMC's West Coast Design Center
- FPGA prototypes functional and being used for code development; Synapse, IBM, RS-232 are well along. H/W verified for Wand and Keyboard wedge, still testing/developing USB.
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)
- BOM status in SAP: N/A

Material Status:

- Placed $10K Engineering fee for metal mask changes due to USB Suspend signal inversion.
- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early September for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date:10 /24/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30~~-5/28~~	Design will be expedited through Hynex
Protos Received	6/22	~~8/9-7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		9/1 ~~8/28~~	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	11/30 ish	
USB Issue Resolution			
USB Trouble shooting	10/19	10/19	Hold time violation detected on 10/18
USB "Fix"	10/26	10/26	UTMC is working on determining net and appropriate fix
USB Parts	11/15	11/15	Assuming metal fix
Proto Acceptance	7/20	11/29	
Major Mfg. Milestones			
Risk Production availability	8/5	10/29 (8/30)	Protos packaged in final package (52 pin PTQFP) – (possible if wafers are shipped direct to packaging fw/o test and drop shipped to Omni in Singapore).
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	11/30	Component Level & S/W
Initial production Start	7/20	11/15	Eight week lead time for production parts

Critical Programmatic Issues:

- UTMC was on site last week – determined root cause of USB issue was a hold time issue.
- UTMC is evaluating how to address USB issue – metal or silicon. It may be possible to screen existing design for reliable USB Operation
- Production parts ship from packaging vendor (ASAT) today – expect tested screened parts on or before 10/29.
- Received additional ICE parts to cover immediate S/W development needs
- Additional material, 25 wafers, has been started and will be staged prior to metal – this will allow any metal fix to be approximately 2 weeks away from a metal change fix.

Design Update:

- Determined USB issue is the result of hold time issue in USB core. Subsequent testing has demonstrated that previously observed USB symptoms are addressed when timing issue is removed (this was done by heating parts – silicon delay extends more than metal)
- Improved Flash programming algorthim developed during UTMC visit
- Evaluating the contingency of placing USB Synapse on Smart Line & NG Hot Shot

Material Status:

- One hundred plus production parts will be available week of 10/29
- Additional 500+ parts available first week in November
- Placed PO for Risk production 6Kparts for September, October, and November
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early September for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 12/5/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/9 ~~7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		9/1 ~~8/28~~	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	1/30 ish	
USB Issue Resolution			
USB Trouble shooting	10/19	10/19	Hold time violation detected on 10/18
USB "Fix"	10/26	10/26	
USB Parts* (initial wafers went past metalization)	11/15	11/15	Screened parts have been available since mid-November
Proto Acceptance	7/20	1/5	
Major Mfg. Milestones			
Risk Production availability	8/5	12/17 (8/30)	These parts will contain all metal fixes for known issues including USB Hold time, power down current, and FLASH controller/programming issues
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	1/15/02	Component Level & S/W
Initial PCB builds - Merlot		12/19/01	Initial build of Merlot scanners tied to "corrected" part availability
Initial production Start	7/20	12/19/01	Eight week lead time for production parts – initial builds will be with "proto" silicon

Critical Programmatic Issues:

- Parts are in metalization. Will then be shipped to ASAT for 2-day turn packaging, then to UTMC (Colorado Springs)
- Fully functional parts with all known defects corrected in metal expected 12/17. Schedule is tight – may meet parts at UTMC in Colorado.

Design Update:

- Identified root cause of USB timing issue – corrected in metal
- Identified root cause of Flash programming issues – corrected in metal
- Identified root cause of excessive suspend current draw – corrected in metal
- Provided full test benches – being converted to test vectors for J750 (Production tester)
- Testing Flash retention limits – saw bit flip on device previously used for ESD testing and early trim parameters/conditioning
- Assembled over 20 functional Merlot/Smart line prototypes to support development

Material Status:

- 25 parts provided for LS 4008 pilot/proto build
- Recently received 32 Flash "conditioned parts" – yields very good
- UTMC is preparing to ship up to 9000 parts by year end
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- Screened chips available to build prototype LS 4008 MLK PCBs 11/30
- PCBs should be available to run in late December for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 12/5/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/9~~7/29~~	Flash in these parts will not be fully operational. (PGA

			ICE parts)
Protos w/functional Flash		9/1 ~~8/28~~	PGA ICE parts with Functional parts Flash
H/W S/W Integration & Testing	8/2	9/3	
S/W Validation	8/30	1/30 ish	
USB Issue Resolution			
USB Trouble shooting	10/19	10/19	Hold time violation detected on 10/18
USB "Fix"	10/26	10/26	
USB Parts* (initial wafers went past metalization)	11/15	11/15	Screened parts have been available since mid-November
Proto Acceptance	7/20	1/5	
Major Mfg. Milestones			
Risk Production availability	8/5	12/21 (8/30)	These parts will contain all metal fixes for known issues including USB Hold time, power down current, and FLASH controller/programming issues
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31	1/15/02	Component Level & S/W
Initial PCB builds - Merlot		12/21/01	Initial build of Merlot scanners tied to "corrected" part availability
Initial production Start	7/20	12/21/01	Eight week lead time for production parts – initial builds will be with "proto" silicon

Critical Programmatic Issues:

- Hand carried, expedited parts arrived at Denver International Airport 5:15 PM EST on 12/19. Parts were then driven to UTMC (Colorado Springs) arrived at 6:30 MST.
- A minimum of 250 fully functional tested parts with all known defects corrected in metal expected 12/21 at Symbol Holtsville. Parts will be screened – Merlot and Chardonay PCBs will be waiting for ASIC arrival.
- Tony Chang and John Fioriglio were at UTMC last week to debug test vectors/test fixture issues. Completed several sets of test vectors while on location and additional vector sets have been brought on line this week.

Design Update:

- Identified root cause of USB timing issue – corrected in metal
- Identified root cause of Flash programming issues – corrected in metal
- Identified root cause of excessive suspend current draw – corrected in metal
- Provided full test benches – being converted to test vectors for J750 (Production tester)
- Testing Flash retention limits – current indications are that problem may be trim value related.
- Assembled over 20 functional Merlot/Smart line prototypes to support development

Material Status:

- 250 parts expected on 12/21.
- Additional 750 pieces expected 1/7/02 or earlier.
- UTMC received 3000 packaged parts 12/19. Additional parts to follow through standard channel.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- Screened chips available to build prototype LS 4008 MLK PCBs 11/30
- PCBs should be available to run in late December for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date 02/14/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
Operations Program Manager:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Rob Lieb, Brad Morris

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Proposed Ramp Plan (monthly):	Product dependent

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23		Startup delays and design mods shifted dates from e-mail schedule by three weeks
Critical Design Review	3/30		
ASIC Proto Fab (start)	4/13		Will need to order qty to cover Alpha/pilot builds
Protos Received	6/22		
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availablity	7/15		
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	7/20		Component Level

Initial production Start	7/20		Eight week lead time for production parts

Critical Issues:

- There are no staffing issues at this time
- Project is progressing, initial H/W design is complete. Now synthesizing gate level design and simulating results. Bringing up FPGA development PCB.
- Schedule is based on one turn of ASIC

Scanner Program Summary

Report Date 02/28/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
Operations Program Manager:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Rob Lieb, Brad Morris

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	UTMC
No. of Top Level Configs:	Numerous -- expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Proposed Ramp Plan (monthly):	Product dependent

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23		UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact.
Critical Design Review	3/30		
ASIC Proto Fab (start)	4/13		Will need to order qty to cover Alpha/pilot builds
Protos Received	6/22		
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availablity	7/15		
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	7/20		Component Level

Initial production Start	7/20		Eight week lead time for production parts

Critical Issues:

- Senior Designer at UTMC had death in family – UTMC has indicated that schedule will take a two to three week delay and will not be ready for final net list until 3/9 - currently working to minimize overall impact with UTMC
- Will need to provide PSC development platform and supporting documentation including H/W spec, System Design Spec (in development). Working with Paul Waxelbaum to coordinate and schedule activities
- Reviewing interface pin-outs for potential damage in incorrect host/ incorrect cable combination is used.
- Project is progressing, initial H/W design is complete. Now synthesizing gate level design and simulating results. FPGA development PCB is functional.
- Schedule is based on one turn of ASIC

Multi Interface ASIC Program Summary

Report Date: 5/9/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Rob Lieb, Brad Morris

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	
ASIC Proto Fab (start)	4/13		Will need to order qty to cover Alpha/pilot builds
Protos Received	6/22	7/27	Late July date includes 2 week expedite fee of $15K (BGA ICE parts)

H/W S/W Integration & Testing	8/2	8/6	
S/W Validation	8/30	8/31	
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availability	8/5		Protos packaged in final package (52 pin PTQFP)
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- 2K plastic parts available in August – Additional 15K parts can be packaged w/ 3week trun-around
- Schedule is based on one turn of ASIC

Design Update:

- Preliminary netlist delivered to UTMC on 3/9/01
- Intermediate Design Review conducted April 12 – minor changes have since been incorporated in I/O circutry
- FPGA prototypes functional and being used for code development
- ASIC in layout – had difficulty with Scan Test insertion, now have >95% coverage
- BOM status in SAP : N/A

Material Status:

- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces,2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early August for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Multi Interface ASIC Program Summary

Report Date: 5/23/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Rob Lieb, Ozgur , Ellen Cordes

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/28	Design will be expedited through Hynex
Protos Received	6/22	7/27	Late July date includes 2 week expedite fee of $15K (BGA ICE parts)

H/W S/W Integration & Testing	8/2	8/6	
S/W Validation	8/30	8/31	
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availability	8/5		Protos packaged in final package (52 pin PTQFP)
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- 2K plastic parts available in August – Additional 15K parts can be packaged w/ 3week turn-around
- Schedule is based on one turn of ASIC

Design Update:

- CDR completed on 5/17 at Aeroflex/UTMC's West Coast Design Center
- Completing final simulations with delay data (SDF) from physical layout
- All changes from Intermediate Design Review conducted April 12 were completed and have been incorporated into design.
- FPGA prototypes functional and being used for code development
- Scan Test insertion complete, now have >95% coverage
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)
- BOM status in SAP : N/A

Material Status:

- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces,2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early August for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 6/6/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs)		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	7/29 ~~7/27~~	Late July date includes 2 week expedite fee of $15K (BGA

			ICE parts)
H/W S/W Integration & Testing	8/2	8/6	
S/W Validation	8/30	8/31	
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availability	8/5		Protos packaged in final package (52 pin PTQFP)
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- 2K plastic parts available in August – Additional 15K parts can be packaged w/ 3week turn-around
- Schedule is based on one turn of ASIC

Design Update:

- Design Database (netlist) transferred to Hynex on 5/29 for fabrication of protos.
- Ran into Scan Test Chain timing issue. Will be addressed in future spin if necessary (on UTMC's nickel) – does not, I repeat, not impact functional performance.
- CDR completed on 5/17 at Aeroflex/UTMC's West Coast Design Center
- FPGA prototypes functional and being used for code development; Synapse, IBM, RS-232 are well along. H/W verified for Wand and Keyboard wedge, still testing/developing USB.
- Scan Test insertion complete, now have >95% coverage. Unfortunately not functional in this spin.
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)
- BOM status in SAP : N/A

Material Status:

- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces,2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.
- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering

- Fixture definition update

Industrial Engineering:

- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:

- PCBs should be available to run in early August for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:

- N/A – Handled at product level

Packaging:

-

Qual:

- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

Scanner Program Summary

Report Date: 6/20/01

Program:	**Multi Interface ASIC**
Description / Key Attributes:	Mixed mode, cored ASIC with Flash, RAM and circuitry to support USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse

Team:

Program Manager:	Peter Musteric
Product Manager:	Various – final product dependent
PCB Process Eng:	N/A
PCB Test Eng:	N/A
F/A Process Eng:	N/A
FA Test Eng:	N/A
Material Program Manager:	N/A
Service Manager/Rep:	N/A
Quality Representative:	N/A
Core Engineering Team Members:	Tony Chang, John Fioriglio, Riz Alladin, Bob DiGiovani, Rob Lieb, Ozgur Keser, Ellen Cordes ....

Design/Mfg.:

Product designed by:	Symbol with specific cells designed by UTMC
Support Responsibility:	Symbol or ? (Product dependent)
Target Mfg. Location:	AeroFlex/UTMC
No. of Top Level Configs:	Numerous – expect in most new scanners including OEM variants for PSC

Marketing:

Critical Market:	Device is applicable to Retail, Industrial and Office
Critical Customers:	PSC
Competitive Product(s):	Synapse
Expected First Year Volume:	Product dependent – 500,000

Product Specifics:

Cost Target (TPC):	$ 3.25	New Technology:	New mixed mode ASIC
Engine/Platform/Scanner:	N/A	Plastic Tooling/Vendor:	N/A
Laser Wavelength/Mfg.:	N/A	Optical Tooling/Vendor:	N/A
Radio/Type/Supplier:	N/A		
Battery:	N/A		
Interfaces:	USB, Keyboard wedge, RS-232, IBM 46XX, wand, Synapse		
ASIC(s):	**Mixed**		
Digital Arch (uP)	Embedded DW51 core (8031 like, used in multiple existing designs).		

List Major PRP Milestones (Gates)	N/A		
Major Design milestones			
Design Kickoff	12/2	12/2	
Preliminary Design Review	12/13	12/13	
Symbol Net list to UTMC	2/23	3/9	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	4/5	
S/W Coding/ and unit test	7/20		Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	3/30	5/17	Completed 5/17 at UTMC West Coast Design Center
ASIC Proto Fab (start)	4/13	5/30 ~~5/28~~	Design will be expedited through Hynex
Protos Received	6/22	8/2 ~~7/29~~	Late July date includes 2 week expedite fee of $15K (BGA

			ICE parts)
H/W S/W Integration & Testing	8/2	8/6	
S/W Validation	8/30	8/31	
Proto Acceptance	7/20		
Major Mfg. Milestones			
Risk Production availability	8/5	8/10	Protos packaged in final package (52 pin PTQFP)
Accessories dates	N/A		
Qual Completion	TBD		Final Product dependent
Rev A Release	8/31		Component Level & S/W
Initial production Start	7/20		Eight week lead time for production parts

Critical Programmatic Issues:

- 2K plastic parts available in August – Additional 15K parts can be packaged w/ 3week turn-around
- Logic sense of USB Suspend signal inverted – corrected in metal layers. Discovered in FPGA proto hours before full reticule set was created. Schedule impact – 3 days
- Schedule is based on one turn of ASIC

Design Update:

- Design Database (netlist) transferred to Hynex on 5/29 for fabrication of protos.
- Ran into Scan Test Chain timing issue. Will be addressed in future spin if necessary (on UTMC's nickel) – does not, I repeat, not impact functional performance.
- CDR completed on 5/17 at Aeroflex/UTMC's West Coast Design Center
- FPGA prototypes functional and being used for code development; Synapse, IBM, RS-232 are well along. H/W verified for Wand and Keyboard wedge, still testing/developing USB.
- Part numbers assigned: 50-13130-057 (Production part), 50-13130-058 (I.C.E. part)
- BOM status in SAP: N/A

Material Status:

- Placed $10K Engineering fee for metal mask changes due to USB Suspend signal inversion.
- Placed $15K expedite fee PO
- Risk production will have to be ordered at prototype time to support other program pilot builds.
- Part cost will be $3.43 @ 500K/year or $3.21 @ 500K/year (1M pieces, 2 year order)

PCB Process:

- Standard surface mount technology (PQFP package)

PCB Test:

- Test Engineering provided preliminary information – will be developed at product level

Final Assembly Process:

- N/A

Final Assembly Test:

- Working with S/W Services & Fixture Design on method for controlling and downloading interface S/W.

- Fixture requests submitted? Program specific – presented overview of device and requirements to Test Engineering
- Fixture definition update

Industrial Engineering:
- Routings/assy instructions/etc progress/issues – N/A Product specific

NPDC PCB Plan Dates:
- PCBs should be available to run in early August for all PSC related products – designs are in process

NPDC Final Assembly Plan Dates:
- N/A – Handled at product level

Packaging:
-

Qual:
- N/A – Handled at product level

Business Data:

Plan\Month	1	2	3	4	5	6	7	8	9	10	11	12
Business Case												
Forecast												
Ramp Plan												

SPD Software Engineering

Symbol's MIF Interface

Robert Lieb, Brad Morris,

Abstract

This document details the interface between the Multi Interface ASIC and the Scanner Subsystem. This document must be used in combination with the Scanner MIA Interface (SMI) document to get a full picture of the communications. This document covers low level communication functionality (the transport) and the flash programming of the MIA. High level communications are discussed in the SMI document.

Revision History

Draft	*Jan. 19 2001*	*Rob Lieb, Brad Morris*	*Draft 1*
D2	*Jan. 31 2001*	*Brad Morris*	*Revised Bus Master, IGD Actions, Scanner Bootstrap Support Requirements*
D3	*Feb 12 2001*	*Brad Morris*	*Update IPCU requirements*
D3	*Feb 13 2001*	*Brad Morris*	*Remove SMI paragraphs, provide reference to SMI document.*
D4	*Feb 22, 2001*	*Rob Lieb, Brad Morris*	*SMI / MIF correlation*

Table of Contents

1 INTRODUCTION **3**

1 Introduction

2 Top-Level System Design

The MIA interface is designed to fit the needs of both low end scanner products (with limited or no flash available) as well as high end scanner products (that conceivably have enough flash space to hold all the interface software).

2.1 Storage of Interface software

2.1.1 Low End Scanners

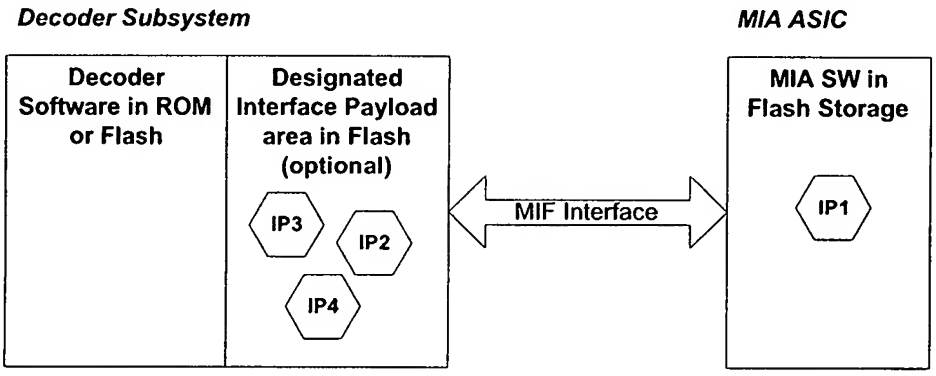
Our present products are sold in one to four product configurations that have a unique combination of hosts: i.e. the LS4007i has USB and Synapse, the LS4005i has IBM Rs485, and Synapse, etc.

In this design, low end scanners would use the flash within the MIA ASIC to store all of its interface software. The flash image that is downloaded into the ASIC is called an Interface Payload, which consists of a bundle of software for one or more interfaces.

Since low end scanners, by definition, do not have storage available for storing multiple interface payloads (in ROM or Flash) only 32640 bytes [=32K bytes -128 bytes] of interfaces can be downloaded into the MIA ASIC's flash at the factory. If field upgrades are required, the scanner must support Flash support utilities for the MIA ASIC. The support center would use a flash utility named IPCU (described later) to update the contents of the MIA ASIC's flash.

2.1.2 High End Scanners

For scanners that have sufficient amounts of flash storage available, the scanner's bootstrap has the option of supporting an "Interface Payload Area" (IPA) to store additional interface payloads.



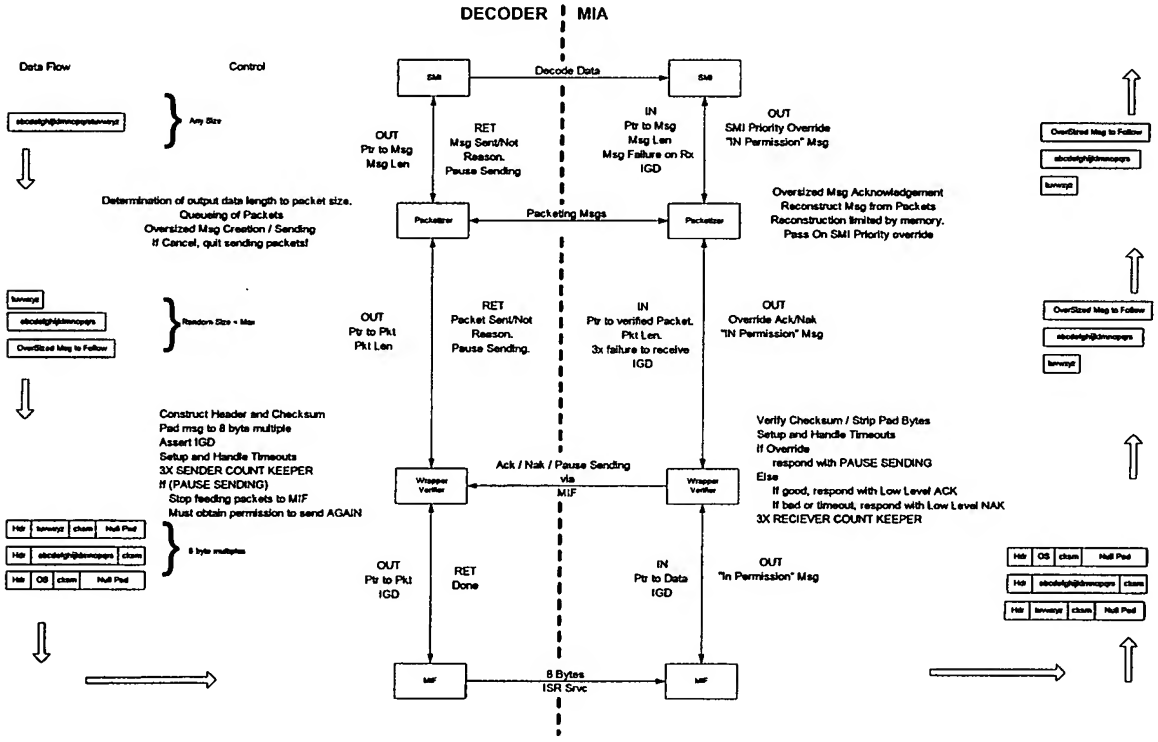
In this type of scanner, both flash areas are taken advantage of. The contents of the MIA ASIC flash holds the interfaces that are available when the scanner powers up. Should

the user select an interface that is not installed in the MIA ASIC flash, the scanner will look at the Interface payload area to find the appropriate payload. At this time, the scanner will program the MIA's flash with the appropriate payload.

2.2 Communication Protocol Layers

Communication between the MIA ASIC and the Decoder subsystem is a via a memory mapped buffer scheme that is called MIF (Mailbox Interface). The Decoder software converses with the MIA using the Scanner MIA Interface (SMI). This interface parallels the familiar SDCI interface on Synapse (with a reduced command set, yet which maintains all of the capabilities). This interface uses the MIF as the low level transport layer. The MIF layer is broken out separately to show that any transport mechanism could be substituted (and it is good programming practice to do so).

A general overview of the protocol layers, the peer to peer transactions and the data flow may be seen in the following figure. This figure is also reproduced at the end of this document in a large format for easy reading!



The MIA is the nominal bus master. That is, the Decoder must request permission to transmit and failing that permission, should not transmit. In fact, the MIA will ignore the decoder's attempted transmission if the decoder is not bus master and the MIA is not expecting some decoder response. The Decoder requests permission to send by asserting IGD (I Got Data). The IGD pin is monitored by the MIA CPU. Permission to transmit is granted by the MIA when it sends the "IN Permission" to the Decoder. Once permission is granted, the Decoder is the temporary bus master. The Decoder can send as many

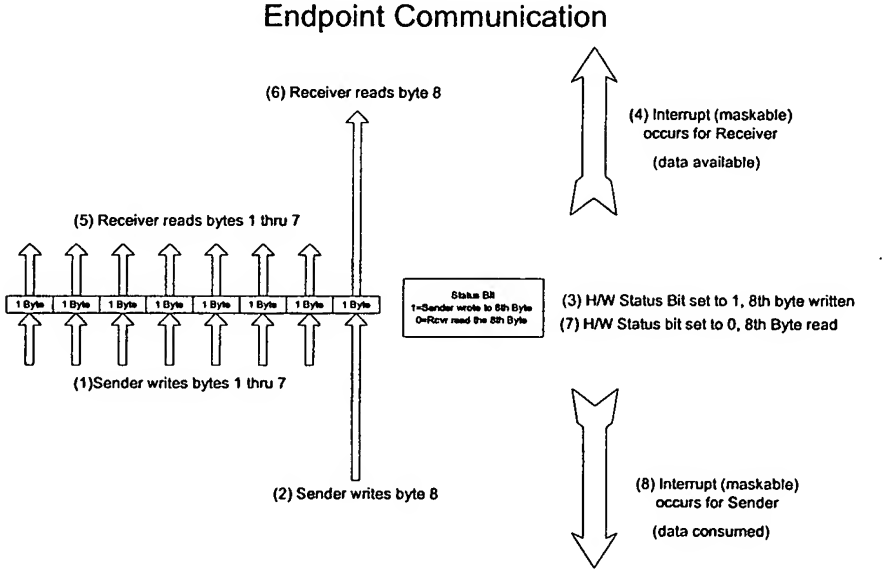
packets of information as it would like. Each packet sent by the Decoder must be acknowledged (at a low level) by the MIA. In the nominal situation, the MIA will permit the Decoder to complete the transmission of all data. Once this occurs, the Decoder will de-assert IGD, thus immediately relinquishing bus master.

If MIA desires to regain bus master status, it sends "pause sending" in reply to a packet. The Decoder will stop sending if it receives "pause sending". Since the packet was not low level ack'd, it must be resent again in the future. Once the Decoder has received the "pause sending", the MIA is bus master and the Decoder becomes the slave again.

2.2.1 MIF Transport Layer

The MIF Transport Layer consists of two endpoints, one for IN the other for OUT. Both function in a similar manner, except for the direction of the data flow.

Each endpoint in the system consists of 8 bytes of memory with a status register and a maskable interrupt signal. All messages are sent in multiples of 8 bytes. Messages shorter than 8 bytes (or multiples of 8 bytes) are padded with zeros to the end. Please consult the following diagram for an explanation of how an Endpoint works. Step (1) The sender places the first byte of the message into mailbox #1. This process continues for the next six bytes, with the end result that 7 bytes are in the first seven bytes mailboxes. The receiver is still completely unaware of any action by the sender. Step (2) The sender places the eighth byte into mailbox #8. This action is the trigger for the subsequent steps which happen automatically in hardware. Step (3) The H/W Status bit is set to 1, indicating that the mailboxes are full, but more specifically that the 8^{th} byte has been written. Step (4) An interrupt occurs on the receiver, if the mask permits. Step (5) The receiver reads the first seven mailboxes. Step (6) The receiver reads the 8^{th} mailbox. This action is the trigger for the subsequent steps which happen automatically in hardware. Step (7) The H/W Status bit is set to 0, indicating that the mailboxes have been read, specifically that the 8^{th} mailbox has been read. Step (8) An interrupt occurs on the sender, if the mask permits.



The MIF transport will send / receive 8 bytes at a time. In the case of the receiver, the first 8 bytes contain the expected length of the message. While the number of bytes received is less than the number indicated, the MIF transport will continue to build a packet until the first occurrence of the number of bytes received is greater than or equal to the expected length.

The mailboxes consist of external memory, within the memory space of both CPUs. This, in combination with the bilateral interrupt scheme, will yield extraordinarily high bandwidth communications.

2.2.2 Wrapper Verifier Layer

The next layer up from the low level MIF transport is termed the Wrapper Verifier Layer. The outbound data is wrapped with the appropriate header, checksum and padding. The inbound data is verified and responded to, then finally stripped of the wrapper.

This layer receives outbound 'bite sized' data from the Packetizer Layer (described below). This layer will construct the actual packet to be sent by the MIF transport layer. The header will be constructed, the raw data will be appended, and then the checksum will be computed and appended. If the final packet size is not a multiple of 8 bytes (required by the MIF Transport), the packet will be zero padded to the next multiple of 8 bytes. Finally, the packet is passed to the MIF Transport layer for sending.

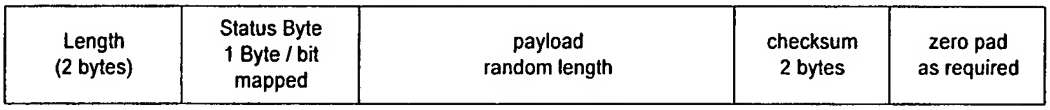
After the packet passes through the MIF Transport, the receiving Wrapper Verifier Layer will verify that the checksum is correct. If it is correct, the receiving Wrapper Verifier Layer will respond with a Low Level ACK (LLACK), indicating that the packet was received correctly. If the checksum computed dynamically does not match the checksum in the received message, then the receiving Wrapper Verifier layer will respond with a Low Level NAK (LLNAK), indicating that the packet was not received correctly.

The sending Wrapper Verifier Layer will send the packet up to and including 3 times total before declaring failure. Similar to the SSI concept, bits within the status byte of the packet will reflect continuation and re-send status.

The Wrapper Verifier layer is also involved in the passing of bus master between the MIA and the Decoder. On the MIA side, once bus master has been granted to the Decoder by "IN permission", bus mastery may be regained by responding with a "Pause Sending" instead of LLACK or LLNAK. On the Decoder side, the Wrapper Verifier will declare immediate failure to send the current packet (to the higher layers) and pass bus mastery back to the MIA. Naturally, in this circumstance, there will pending data from the Decoder and IGD should remain asserted. Once the MIA has finished with the transaction that caused the "Pause Sending", the MIA will note that IGD is asserted and pass control of the bus back to the Decoder.

PACKET FORMAT

All data sent at the Wrapper Verifier layer has the following format. The length is the number of bytes of Packet Data including the packet length bytes (but not including the 2 byte checksum) A 16 bit checksum is used to verify packet integrity. If the packet length overall (including the checksum bytes) is not an even multiple of 8 bytes, the packet will be zero padded AFTER the checksum to obtain the next 8 byte multiple.



Length: (two byte field size) number of bytes, including itself, up to but not including the checksum. It also does NOT include the zero pad bytes (if present). The receiving MIF transport shall use this to recreate packets. Please note that while this implies that the maximum message length is 65535 bytes, as a practical matter, the maximum message length will be smaller and agreed to during Scanner / MIA Initialization. Since the current size of RAM in the MIA is constrained to 1024 bytes, and will include such things as the stack and variables, the maximum message length will range downwards from 1024, and is more likely to be in the several hundred bytes size.
Status Byte: (one byte field size) One bit indicates if a re-send (or not). Another bit indicates continuation packet (or not).
Payload: The actual data content which is being transmitted. SMI messages will be placed here, intact, without change.
Checksum: (two byte field size) 16 bit twos complement checksum.
Zero Pad: As required to make overall packet length a multiple of 8 bytes. That is, this field is zero to seven bytes long, and the content of any byte in this field is "00".

2.2.3 Packetizer Layer

This layer shall receive arbitrary length data from the SMI layer (described later) and send this data to lower layers broken up into packet payload 'bite sized' lumps. That is, if the largest packet that can be safely sent between the Decoder and the MIA (or visa versa) is 80 bytes, then the Packetizer Layer will break larger messages into 75 byte payloads (leaving enough room for the wrapper). To make this data intelligible on the receiving Packetizer Layer, it shall be the responsibility of this layer to send an "Oversized Message to Follow message" prior to sending the actual data which must be broken up.

For example, suppose that the data to be sent is 100 bytes long, and the max packet size is 80 bytes. The Packetizer Layer will first send an "Oversized Message to Follow" message to the MIA Packetizer Layer, indicating that 100 bytes of payload are to follow.

The Decoder's Packetizer Layer will then send the first 75 bytes to the Wrapper Verifier Layer, which will construct a packet from that payload, the final size of that packet will be 80 bytes (including the checksum). This will be passed to the MIA Packetizer Layer, which now knows that there are another 25 bytes of data payload to follow. After the handshake from the Wrapper Verifier, the Decoders Packetizer Layer will send the remaining 25 bytes to the Wrapper Verifier. The reconstruction of the overall data message from packets will be limited by available memory.

If the payload will fit into one packet without packetization, then this layer shall merely pass on the data without modification.

2.2.4 Bus Master Arbitration

In a well behaved MIA / Decoder system, the Decoder will assert IGD when it has data to send. At the earliest opportunity, the MIA will grant bus master to the Decoder via "IN permission" (note that this correlates with the SMI 'Packet Control' message). The assertion of IGD will occur by the Wrapper Verifier layer. The Decoder application will pass a pointer to the data to be sent to the Decoder SMI layer. This, in turn will be passed to the Decoder Packetizer layer and again in turn to the Decoder Wrapper Verifier layer, each layer performing the actions previously described. When the first packet is ready to be passed through the mailboxes, the Wrapper Verifier layer shall assert IGD. Thus, when the "IN Permission" is granted, the packet is sent immediately. If there is another packet to send, the Wrapper Verifier layer shall keep IGD asserted. If no more packets are to follow, the Wrapper Verifier shall de-assert IGD.

The Decoder has two scenarios to watch. The simple scenario is that the Decoder sends absolutely everything that it needs to. Once all the data is sent (and low level ack'd), the Decoder Wrapper Verifier layer should de-assert IGD. In doing so, the Decoder immediately relinquishes bus master. The other scenario is when the MIA issues a "Pause Sending" in response to a packet. The MIA grabs bus master, precluding the Decoder Wrapper Verifier from re-sending the packet. Here, the IGD remains asserted (since there remains data to be sent, i.e.> it was not low level ack'd) and the MIA will re-grant "IN permission" sometime later.

A poorly behaved MIA / Decoder system will have IGD asserted, even though there is NO data to send. The MIA will not be aware of this fact and will grant "IN Permission" to the Decoder. There is no data to send, yet the Decoder has bus master at this point. The Decoder should first de-assert IGD, then issue a null message, indicating that there is no data and permit the MIA to regain bus master.

A very poorly behaved Decoder will not de-assert IGD. This behavior appears, at first glance, to be a method of retaining bus mastery for the decoder. This places the MIA in the untenable position of being a slave to two masters (the Decoder and the External Host). Once "IN Permission" has been granted to the Decoder, the Decoder has 3

milliseconds to complete the transmission of the packet. Each subsequent packet has 3 milliseconds to complete, the time starting from the receipt of the LLACK / LLNAK by the Decoder Wrapper Verifier layer. Failure to do so will cause a timeout. The MIA Wrapper Verifier shall then issue a "pause sending", which in turn will cause bus master to revert to the MIA. Naturally, the MIA will sense that IGD is still asserted and grant "IN Permission" again. Should this continue for multiple permissions without data actually being passed, the MIA system will take corrective action, up to and including a power on reset of the Decoder system.

2.2.5 SMI Interface

The SMI Interface uses the MIF Interface to transport its messages. Please consult the SMI Interface document for details of how that interface uses this transport to communicate.

2.3 Flash Utility (The Interface Payload Configuration Utility)

The MIA is a configurable ASIC. The configurable nature of the device will require support functionality. The support functionality will be required within the context of the scanner bootstrap, within the decoder application and within the user's PC. The software that runs in the PC is known as the Interface Payload Configuration Utility (IPCU).

The IPCU must function within the context of a Windows environment and be, in fact, a windows executable. The current demo of the IPCU has a Windows Explorer feel, since users are normally familiar with this layout.

The support functionality within the scanner bootstrap consists of read / write access to the Interface Payload Area (IPA) and to the MIA Flash memory . Other details regarding these areas will also be accessible, for example, max size.

The support functionality within the decoder application will consist of read / write access to the MIA flash part.

2.3.1 Requirements

The IPCU must be able to determine what Interface Payloads (here in after IP's) are available. It shall be the responsibility of the IPCU to certify that the Libraries and the IP's conform to the format specified in this document.

2.3.1.1 IP Sources

IP's will be available from many sources, which can be:

A) IP's linked into the Decoder application software.

These IP's will remain constant throughout the life of the decoder application. They cannot be changed or overwritten by the IPCU. These IP's must conform to the format defined within this document. These IP's will not be a source for the IPCU to install a host, but can be a source for installing payloads from within the context of the decoder application.

Most probably, this will be used as default payloads, for error conditions which are non-recoverable without scanner reconfiguration.

B) IP's in a library in the Interface Payload Area (IPA) in the scanner

The IPA is a section of flash reserved for IP's. This is configurable and can be overwritten by the IPCU, as required. Libraries loaded into this area must conform to the format specified within this document.

The IPA must also contain an allocation table, that distinguishes those areas that are allocated (used) within the IPA and those areas which are not allocated (used). Further, the table should indicate the start pointer to each entry in the IPA. This start pointer will bring us to the start of a library (see library layout) or to the start of an IP (see IP layout). Similar to a file allocation table for a hard drive, the IPCU must maintain the memory allocated (used) in the IPA. Therefore, multiple libraries and multiple IP's can be stored into one IPA, to the limit of the maximum number of bytes available.

The IPCU can determine the content of every byte in the IPA and the size of the IPA. The IPCU does not know physical addresses, rather it knows relative addresses within the context of the IPA.

C) IP installed as the MIA host.

Both a source and destination, this flash is contained within the MIA part and is write-able by the IPCU. It will be considered to be a source for backups and a destination for the Installed Host.

Only one IP can be stored here, however, this IP may be an executable which contains multiple hosts, similar to our current host selection paradigm.

D) IP's individually available from the local disk, which consist of scanner backup and user constructed libraries

Users may create backups or custom Libraries. This portion of the IPCU will investigate the network neighborhood (at user direction) for those libraries and/or backups. Since these will have been created by the IPCU, they will conform to the required format

E) IP's and libraries available from the Symbol Technologies web page, which will have the 'latest and greatest'.

The IPCU shall access our new web page which will have the latest version of executable MIA code for each interface. Prepackaged Libraries will also be available, such as a retail library.

2.3.1.2 Sizing Requirements

The IPCU must also determine the size of the IPA and the available size of the MIA flash in bytes. Support functionality within the scanner bootstrap will support this sizing requirement. The IPCU will prohibit the download of IP's or Libraries which will not fit in the designated destination area. That is, should the user attempt to fit a 65k IP into the MIA flash, the IPCU will prohibit the activity prior to writing the first byte into the MIA flash. Similarly for the IPA, the IPCU will prohibit writing to the IPA unless the object which is being written will fit. Informative messages will be displayed to the user, urging corrective action. The original contents of the IPA or the MIA flash shall remain unchanged in this scenario.

2.3.1.3 Date Time Revision Functionality

Upon connection with the scanner, the IPCU will determine the currently installed IP's in the three storage areas (the decoder application, the IPA and the MIA flash) and will determine the revision of the IP's as well as the creation date and time of the IP's The IPCU will compare the revision date time to the web based, Symbol Technologies maintained latest IP's and inform the user which IP's are out of date. Users will not be required to update to the latest revision, however, they must be informed of the 'out of date' nature of IP's that they are dealing with.

2.3.1.4 Backup and Restore Functionality

The IPCU must be able to back up the IP's and Libraries that are in the Scanner. The backup method shall create re-installable IP's and Libraries from the raw data retrieved from the scanner. The source in the scanner may be from any one of the IPCU accessible storage areas (includes the MIA Flash and the IPA, does not include IP's linked into the decoder application). The destination of this backup shall be a user designated file, on the host PC where the IPCU is executing.

The IPCU shall then be capable of using these backup files to restore the IP's and Libraries to the scanner. There shall be no notice-able artifact remaining from this restoration. That is, if we take a full flash memory image before and after the restoration, there shall be NO differences.

Note that the IPCU will be required to maintain the revision date time information within the backup in the same format as other IP's.

2.3.1.5 Library Creation Functionality

The IPCU must be able to create new Libraries of IP's, from existing individual IP's, independent of source. That is, the IPCU will provide a facility for the capture and bundling of individual IP's into a Library. The created Library must conform to the

layout contained within this document. The created Library must be capable of being installed into the IPA and used directly by the other functionality demanded of this document.

2.3.1.6 New Host Installation (by IPCU)

The IPCU must be able to install a new host in the MIA architecture. The User will designate the host to be installed. The IPCU must be capable of installing this host, considering the source to be any one of the following: (1) IPA (2) Locally available IP's (3) Locally available Libraries, taking one of the IP's in the library (4) Symbol Technologies maintained web page of IP's and Libraries.

2.3.1.7 New Host Installation (by Decoder)

It is required that the Decoder be able to install a new host to the MIA architecture, via scanning a parameter barcode. That is, it is critical that the user be able to select an interface WITHOUT the IPCU being available. This implies that the Libraries and IP's maintained by the IPCU conform to the layouts in a strict manner, so that the decoder can depend upon the structures and IP's as found within the previously denoted areas.

2.3.2 Scanner Requirements

The command set to support re-flashing the MIA flash part must reside within the decoders' bootstrap. That is, with the Flash Download cable installed, the MIA CPU is held in reset and will not function. The IPCU will communicate with the Decoders' bootstrap, which can access the MIA flash directly for reads and writes.

Consistent with the requirement that the Decoder install a new MIA host via barcode scanning, the decoder application must also support read write capability to MIA flash part.

2.3.3 Interface Payload Change Requirements

During the life cycle of the MIA, Interface Payloads will occasionally change. It will be the responsibility of the Agent of Change (IPCU, Decoder, etc) to update the special 128 bytes of NVM at the highest addresses of MIA memory, at the time of IP update.

This NVM block contains several parameters which are required for MIA functionality.

2.3.3.1 Default Host

One parameter is the Default Host. Each IP has at least one host, but typically several are present. This parameter indicates which host is the default, for the installed IP.

2.3.3.2 Installed IP Designation

This parameter shall detail the three letter name of the installed IP.

2.3.3.3 Serial Number

Another parameter is a 6 byte unique serial number. This serial number is programmed in the Symbol Technologies factory and is unique for each MIA part programmed. This number has several purposes. One, it is the unique USB number required for proper USB communications. Two, it can and will provide a method for Customer Service to identify revisions in hardware! Other functions may use this number, but shall not change it.

The Agent of Change must read the serial number prior to change, store it and then restore it at the write phase of operation. Since this number must be unique for USB and indirectly identifies the hardware revision, this number must not be changed.

Upon change in this 128 byte sector, it will be required first to erase the 128 bytes, then write the new values and finally install the sector checksum. It shall be the responsibility of the IPCU to verify that the serial number is correct (via read and compare with the earlier stored number) in this page PRIOR to installing the sector checksum. In this manner, if the user prematurely 'pulls the plug' an incorrect serial number will not be accepted!

2.3.3.4 Country Code

Another parameter is the country code used by USB.

2.3.3.5 IP Start Address, Stop Address and Checksum

This three value bank shall hold a pointer (inclusive) of the start address of the IP, a pointer (inclusive) of the stop address of the IP and a Twos complement 16 bit (2 byte) checksum of the loaded IP. Note that when the stored checksum is added to the computed checksum, the result shall be zero. This will permit verification of the installed IP. Proper verification shall also include the guarantee that the area constrained by the start and stop pointers is non-zero. Verification shall also guarantee that the start address is lower in memory than the stop address, that is, they cannot point to the same location in flash and they cannot be crossed where the stop is before the start.

2.3.3.6 IP Freshness Date

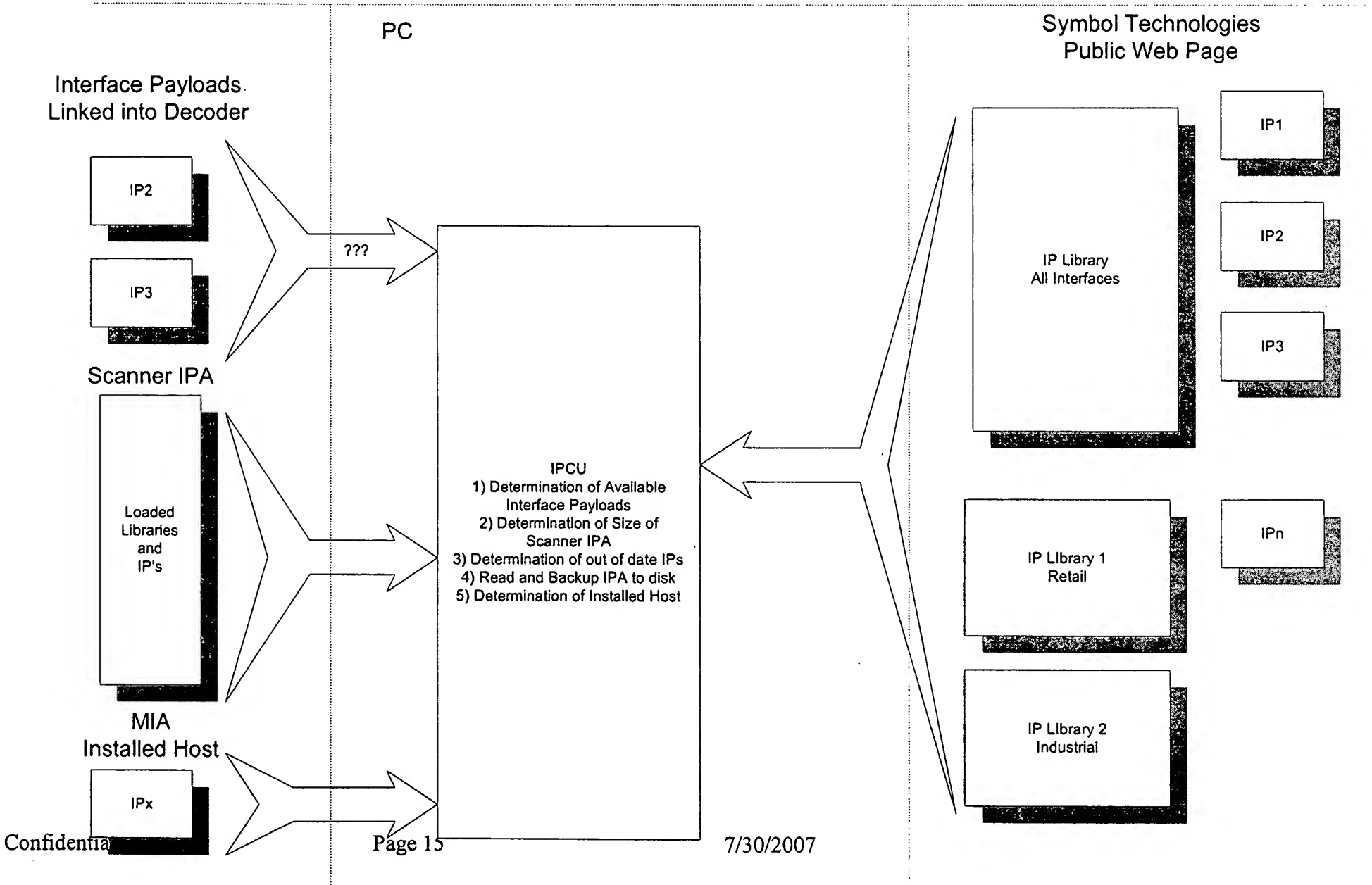
As the MIA architecture matures, the IP's initially intended for the MIA will be supplanted by IP's of later revision. Since the names of the IP's relate to the Interface type (and do not contain revision information) it will be necessary to store revision information elsewhere. The date/time of the creation of the IP (not the date it was stored into the MIA flash part) shall be maintained here. An additional 16 bytes will be reserved for a free form revision string.

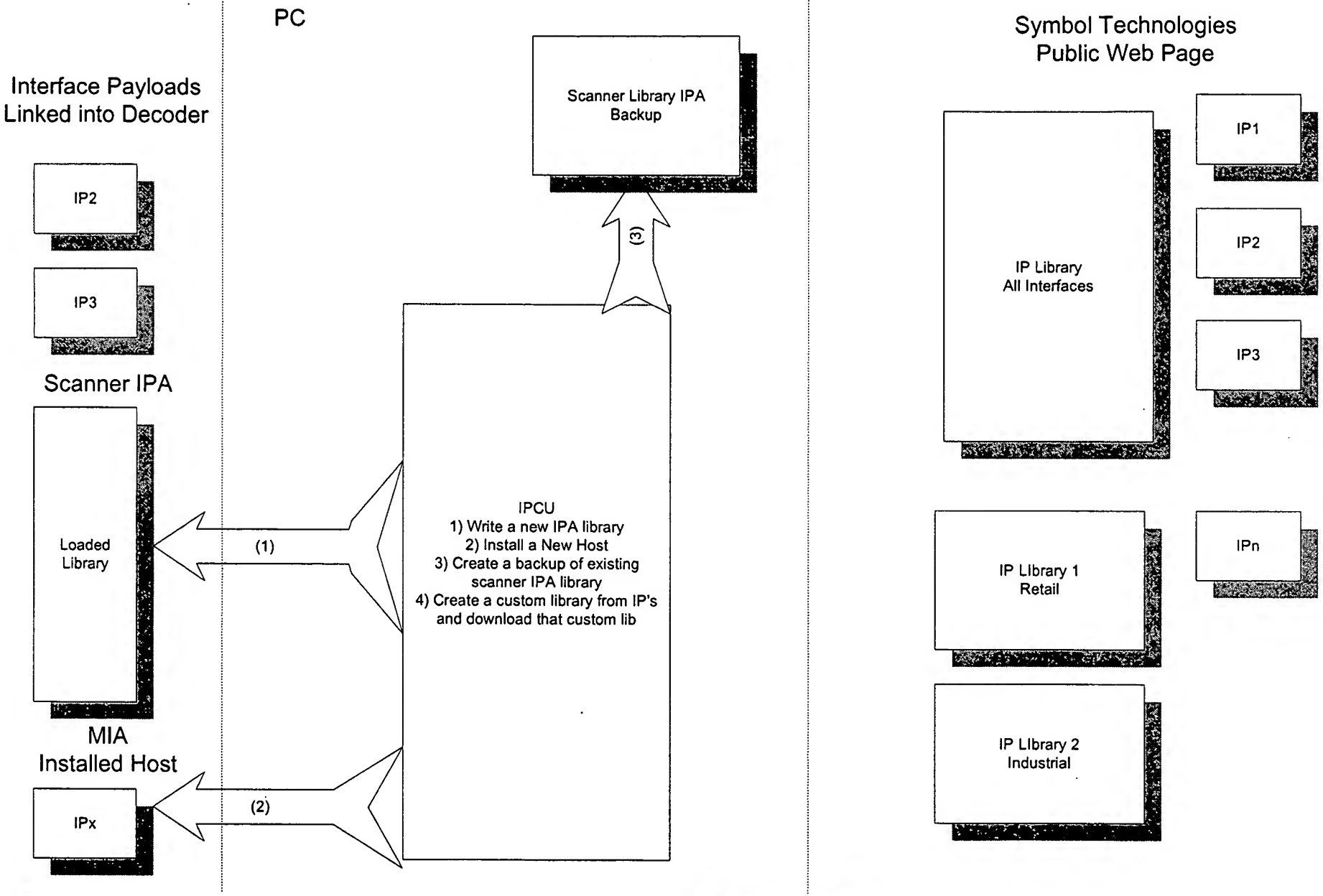
2.3.3.7 Top "128 Byte Sector" Checksum

This twos complement 16 bit checksum, when added to the sum of the other 126 bytes of NVM in this 128 byte sector, shall yield a sum of zero.

Upon power up, the MIA software shall verify that the checksum of this 128 byte sector is correct. If it is incorrect, it shall be assumed that the serial number (6 byte value detailed earlier) is correct and carried forward as is. That is, the utilities that will correct the 128 byte sector area will merely read the serial number contained and write the number read back upon restoration, without change.

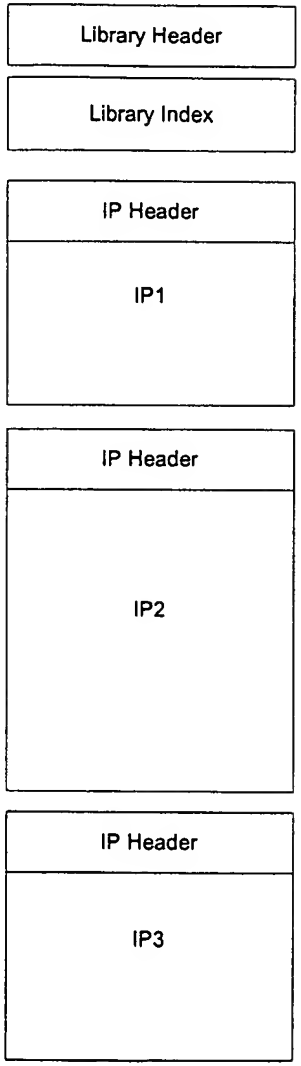
IPCU Determination of Characteristics




PC
Interface Payloads
Linked into Decoder
IP2
IP3
Scanner IPA
Loaded
Library
MIA
Installed Host
IPx
(1)
(2)
(3)
Scanner Library IPA
Backup
IPCU
1) Write a new IPA library
2) Install a New Host
3) Create a backup of existing
scanner IPA library
4) Create a custom library from IP's
and download that custom lib
Symbol Technologies
Public Web Page
IP Library
All Interfaces
IP1
IP2
IP3
IP Library 1
Retail
IPn
IP Library 2
Industrial

IP Library Layout

One contiguous block of bytes



Library Header

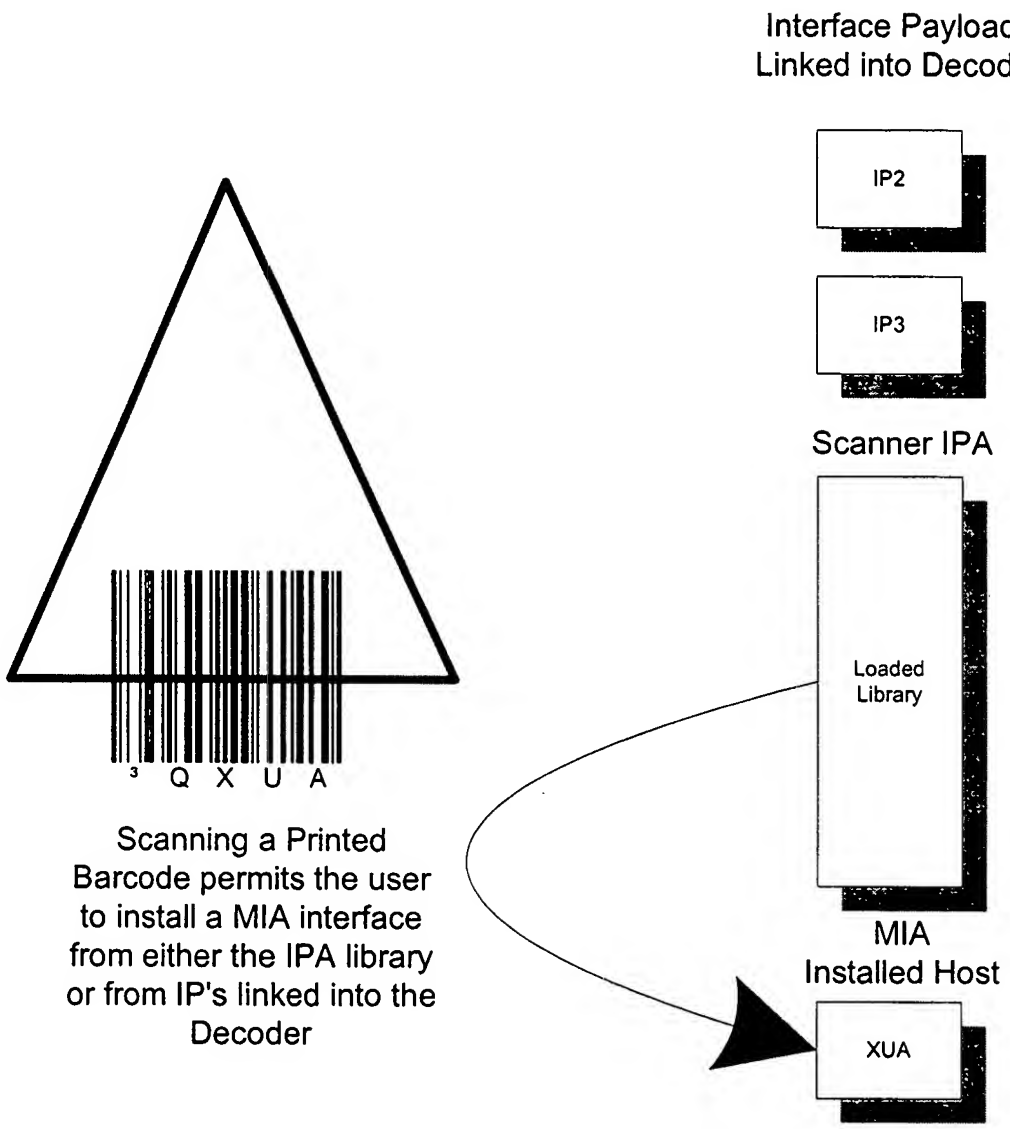
LIbrary Name	Library Length	Library Checksum

Library Index

Three Letter Name	Start Pointer
Three Letter Name	Start Pointer
Three Letter Name	Start Pointer
End Marker	

IP Header

Length	16 bit Checksum
IP Name 3 Letter	
Revision / Date String	


Interface Payloads
Linked into Decoder
IP2
IP3
Scanner IPA
Loaded
Library
MIA
Installed Host
XUA
3 Q X U A
Scanning a Printed
Barcode permits the user
to install a MIA interface
from either the IPA library
or from IP's linked into the
Decoder

Interface Decoder / PC
Special IP Download Cable Installed

- Read / Write : MIA Installed Host Area
  - Offset from Start, #of Bytes,Data CRC,Data Bytes - EXCLUDES MSG WRAPPER
  - Can be used to read:
    - Installed Host Name
    - Freshness Date
  - Used by PC to Backup Scanner
- Read / Write to IPA in Scanner
  - Offset from Start, #of Bytes,Data CRC,Data Bytes - EXCLUDES MSG WRAPPER
  - Can be used to read:
    - Installed Library Name
    - Library Content (IP's, Dates, Sizes, Etc)
  - Used by PC to Backup Scanner
- Read IPA Size in Scanner
- Read Installed Host Size in Scanner

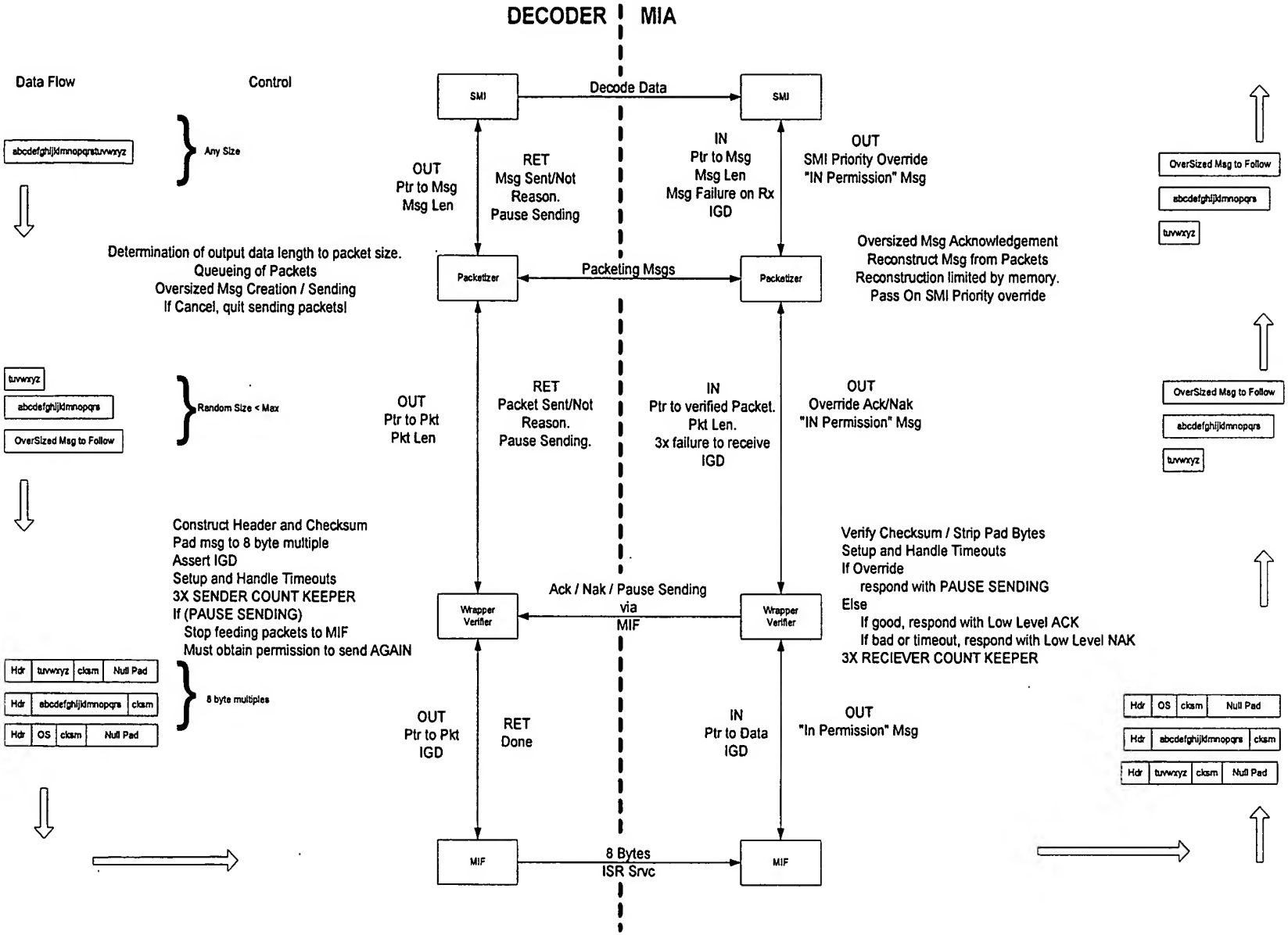

DECODER
MIA
Data Flow
Control
abcdefghijklmnopqrstuvwxyz
Any Size
SMI
Decode Data
SMI
OUT
Ptr to Msg
Msg Len
RET
Msg Sent/Not
Reason.
Pause Sending
IN
Ptr to Msg
Msg Len
Msg Failure on Rx
IGD
OUT
SMI Priority Override
"IN Permission" Msg
OverSized Msg to Follow
abcdefghijklmnopqrs
tuvwxyz
Determination of output data length to packet size.
Queueing of Packets
Oversized Msg Creation / Sending
If Cancel, quit sending packets!
Packetizer
Packeting Msgs
Packetizer
Oversized Msg Acknowledgement
Reconstruct Msg from Packets
Reconstruction limited by memory.
Pass On SMI Priority override
tuvwxyz
abcdefghijklmnopqrs
OverSized Msg to Follow
Random Size < Max
OUT
Ptr to Pkt
Pkt Len
RET
Packet Sent/Not
Reason.
Pause Sending.
IN
Ptr to verified Packet.
Pkt Len.
3x failure to receive
IGD
OUT
Override Ack/Nak
"IN Permission" Msg
OverSized Msg to Follow
abcdefghijklmnopqrs
tuvwxyz
Construct Header and Checksum
Pad msg to 8 byte multiple
Assert IGD
Setup and Handle Timeouts
3X SENDER COUNT KEEPER
If (PAUSE SENDING)
Stop feeding packets to MIF
Must obtain permission to send AGAIN
Ack / Nak / Pause Sending
via
MIF
Wrapper
Verifier
Wrapper
Verifier
Verify Checksum / Strip Pad Bytes
Setup and Handle Timeouts
If Override
respond with PAUSE SENDING
Else
If good, respond with Low Level ACK
If bad or timeout, respond with Low Level NAK
3X RECIEVER COUNT KEEPER
Hdr
tuvwxyz
cksm
Null Pad
Hdr
abcdefghijklmnopqrs
cksm
Hdr
OS
cksm
Null Pad
8 byte multiples
OUT
Ptr to Pkt
IGD
RET
Done
IN
Ptr to Data
IGD
OUT
"In Permission" Msg
Hdr
OS
cksm
Null Pad
Hdr
abcdefghijklmnopqrs
cksm
Hdr
tuvwxyz
cksm
Null Pad
MIF
8 Bytes
ISR Srvc
MIF

EXHIBIT J

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DOCUMENT TITLE:

MULTI-INTERFACE ASIC SPECIFICATION

DOC. NO:	SHEET 1 OF 54 REVISION : A

TABLE OF CONTENTS

1 Revision History 4
2 Conventions 4
3 Reference Documents: 5
4 Glossary and Definitions 5
5 Application 6
6 Block Diagram 6
7 I/O Pin Definition 9
8 I/O Pin Definition for the Special Chip 12
9 The DC Specification 14
10 PLL Clock Generator 14
11 Charge Pump 14
12 USB SIE 15
13 Processor 16
14 USB Transceiver 16
15 Bus Interface 18
16 DMA Controller 22
17 Clock Generator 25
18 Mailbox I/O Block 26
19 FLASH ROM/Static RAM 29
20 FLASH ROM Programming 30
21 UART 33
22 OCIA 33
23 Programmable Interval Timer 35
24 Watch Dog Timer 35
25 USB Control and Configuration 36
26 I/O Interrupts 37
27 I/O Control Logic Block 38
28 Interface Control 41
29 Interface Decode Logic 41
30 I/O Mux-Analog PHY 42
31 RS-232 I/O Specification 44
32 RS-485 I/O Specification 45
32.1 Pin Name Definitions 45
33 The Differential Receivers 46

34 The Discrete Drivers and Receivers 504746
35 The Analog Switches 514847
36 Status indicator LED driver 524948
37 Power down and Wakeup Detector 524948
38 Download Detector 555251
39 3.3V Regulator 555251
40 Development Tools 555251
41 Fault Coverage 555251
42 Package 575453
43 Marking 575453
44 Temperature Range 575453
45 Compliance 575453
46 ESD 575453

LIST OF FIGURES

Figure 1. Multi-Interface Block Diagram 7
Figure 2. Chip Outline 8
Figure 3. Chip Outline of Special Bond out Chip 111111

1 Revision History

Revisioin	Issue Date	Comment
1		First draft 5/1/2000 TC
2		Added LED drivers and updated bus specifications 5/11/2000
3		Changed the USB controller to a generic controller with SIE and UART timer plus OCIA interface
4		Changed the controller to a 8051 core Modified the mailbox to 8 slots 1/14/01 Revised the I/O control and the USB tranceiver spec. 1/23/01
5		Corrected few errors in the spec. 2/12/01 Modified the wake up detection section to eliminate the 32KHz clock in suspend mode. Added pull-up resistor on RESET and CS, and pull-down resistor on FWE. Added the PSEN signal on the ICE version. Changed the cap. To 0.22uF on charge-pump. Added the low-power control on RS-232 output.
6		Changes made on the Digital I/O to be 3.3V and 5V tolerant. An I/O pin was spared to be the VCCIO to bring I/O voltage to the chip. Signal name changed as the following: A0 -> CMD/DATA SUSPEND -> SCAN_PWR_EN SCANSTAND -> WAKEUP_IN RSV2 -> POF_INT RSV3 -> VCCIO WAKEUP -> WAKEUP_OUT
7		Changed the RS-232 output resistance to 245-ohm min. Corrected the I/O directions for TXD_BY and RXD_BY. Change signal name SYN_CLK to USB_DET/SYN_CLK. Corrected few clerical errors on page 38. Changed SCAN_PWR_EN to SCAN_PWR_EN*

2 Conventions

1. All voltage specifications for input/output pins are referred to GND, unless otherwise specified.

3 Reference Documents:

The IBM-AT Hardware Technical Reference Manual

Maxim MAX1485 Data Sheet.

Analog Devices ADM101E Data Sheet.

Micrel MIC2550 Data Sheet.

Philips PDIUSBD12 Data Sheet.

Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange (ANSI/TIA/EIA-232-F-1997)

USB 1.1 Specification

Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems (ANSI/TIA/EIA-485-A-98)

NCR 250-0006186 OCIA Interface Document

4 Glossary and Definitions

RS-232	The EIA standard was adopted in 1975 for serial data communication. It is a common communication interface standard that permits DTEs and DCEs to connect successfully.
RS-485	It is similar to RS-232 except it uses a balanced (differential) media and carries signal in both directions.
Charge Pump	A way to convert/invert DC voltage by using switches or diodes.
Synapse	This is a bi-directional serial interface.
Wand Emulation	As it seems, it is to emulate the old Wand bar-code reader. It consists of a clock signal along with digital bar-code pattern. This is a unidirectional serial interface.
Keyboard Wedge	The keyboard plugs into the wedge and the wedge device plugs into the computer where the keyboard was.
USB	Universal Serial Bus is a serial communication standard.
OCIA	Optically Coupled Interface Adapter is a bi-directional serial interface. It uses clocks to synchronize data during communication. The clock is always originated from the receiving (Host) end.
UART	Universal Asynchronous Receiver Transmitter.
PPIA	Programmable Parallel Interface Adapter.

5 Application

The chip is going to be used in a POS device to provide greatest adaptability toward different I/O functions. In addition, it fits all I/O configurations in a 10-pin connector. There are two versions of chips specified herein. One is the normal chip without additional test pads and the other is the special package chip with extra pins for using with an 8051 In-Circuit-Emulator.

6 Block Diagram

The detailed block diagram of this multi-interface controller ASIC is depicted in the following diagram. It accommodates seven different I/O functions. The internal 8051 processor can select any one of these seven interfaces. ~~Eight out of ten connector pins are shared among these interfaces~~The interface pins were designed to multiplex TTL, RS-232 level, and 3.3 volt differential signalling. The required I/O signals for each function are:

USB:	D+, D- inout;
RS-232:	TXD, RTS out; RXD,CTS in;
RS-485:	IBM+, IBM- inout;
KBD Wedge:	KBD_CLK, KBD_DAT inout; TRM_CLK, TRM_DAT inout;
Synapse:	SYN_CLK, SYN_DAT inout;
Wand Emul.:	WAND_RTS, WAND_DBP out; WAND_CTS in;
OCIA	OCIA_SDATA,OCIA_CLKIN, OCIA_CLKOUT in; OCIA_RDATA out;

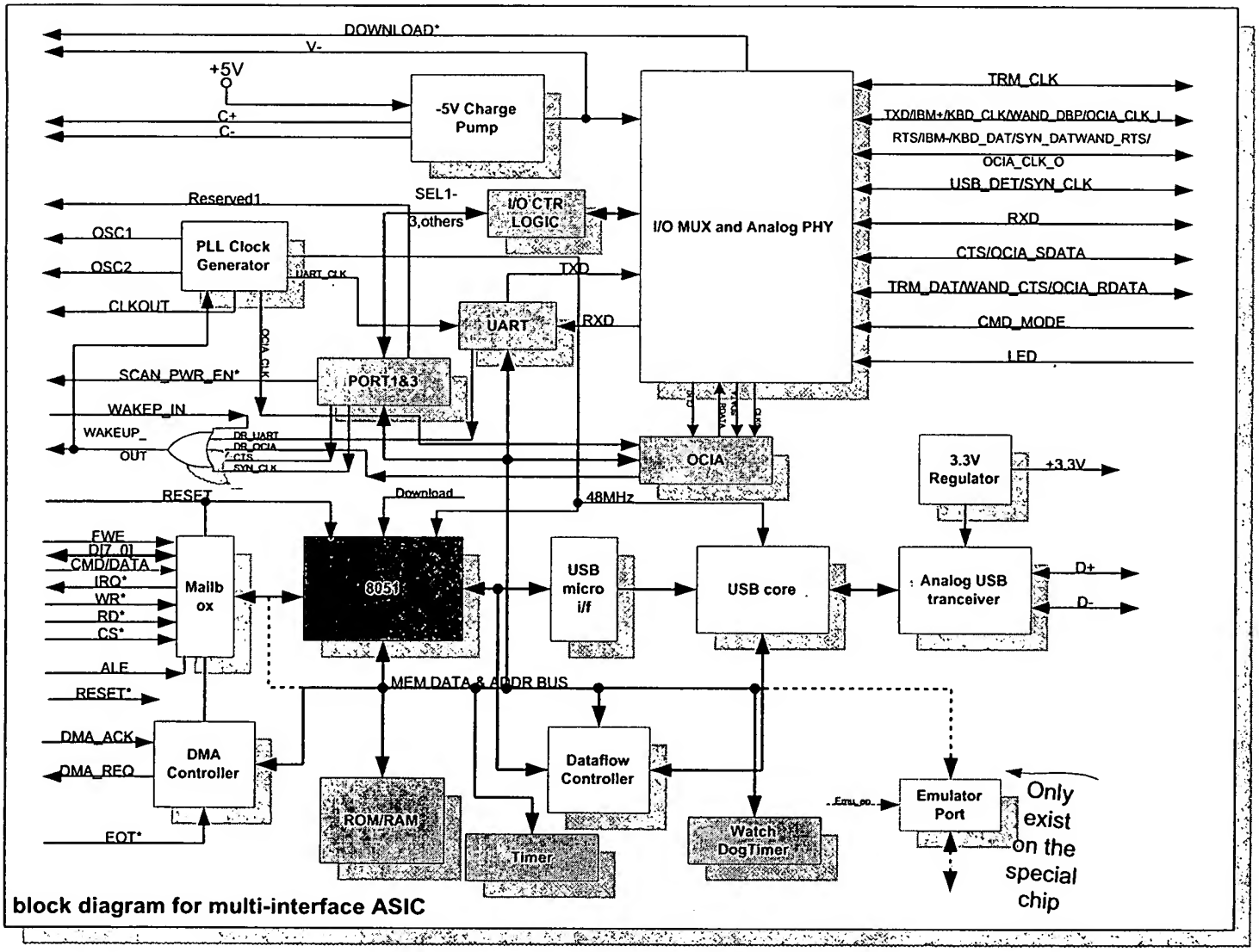


Figure 1. Multi-Interface Block Diagram

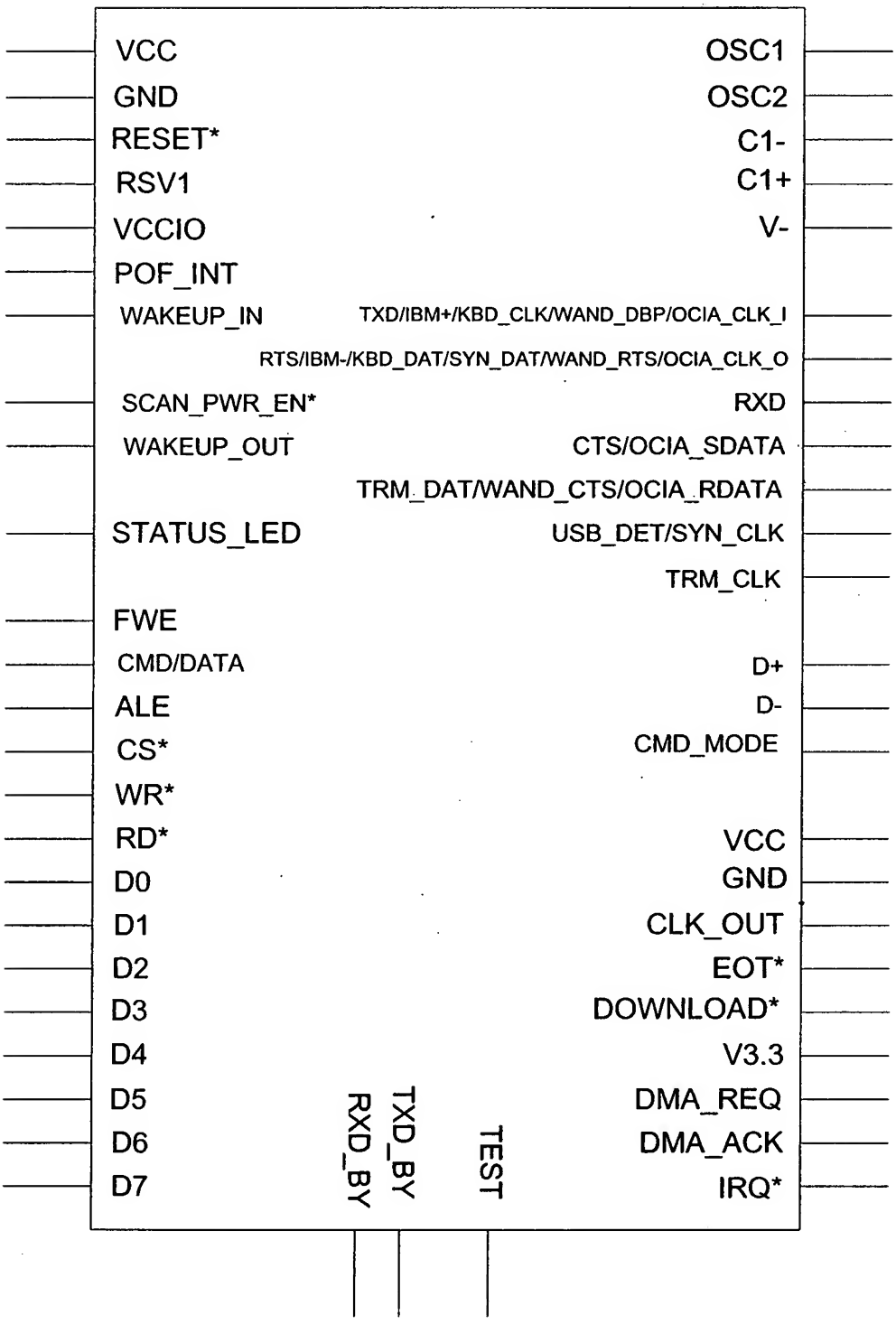


Figure 2. Chip Outline

7 I/O Pin Definition

Pin Name	Dig/Ana	In/Out	No. Pin	Description
VCC	Power		2	Nominal +5V
GND	Power		3	Ground
C1+			1	positive side of voltage inversion capacitor
C1-			1	negative side of voltage inversion capacitor
V-			1	-5V output out of charge pump
V3.3	Power	Out	1	Regulated 3.3V out
WAKEUP_OUT	Digital	Out	1	
TEST	Digital	In	1	Dedicated test pin
~~Spares~~RSV1	Digital	In/Out	1	Spare ~~PPIA~~ 8051 port pin output for future use
VCCIO	Power	In	1	Digital I/O cell power supply
POF_INT	Digital	Out	1	POF interrupt
ALE	Digital	In	1	Address latch enable, used on multiplex address/data mode
WAKEUP_IN	Digital	In	1	External Wakeup input (for wakeup)
OSC1-2	Passive		2	Crystal inputs or Resonator inputs
D0-7	Digital	In/Out	8	8-bit data bus
RD*	Digital	In	1	Read Strobe
WR*	Digital	In	1	Write Strobe
FWE	Digital	In	1	Flash Write Enable
CMD/DATA	Digital	In	1	CMD (Aaddress)/Data signal ~~indicator~~ used ~~o~~in non-multiplex mode.
CS*	Digital	In	1	Chip Select
SCAN_PWR_EN*	Digital	Out	1	Scanner Power Enable control
RESET*	Digital	In	1	Master Reset
EOT*	Digital	Out	1	End of DMA transfer
D+	Analog	In/Out	1	USB Differential Positive out
D-	Analog	In/Out	1	USB Differential N~~n~~egative out
TXD/IBM+/KBD_CLK/WAND_DBP/OCIA_CLK_I	Analog	In/Out	1	RS-232 TXD/485 Differential Pos/Keyboard clock/Wand DBP/OCIA clock in
RTS/IBM-/SYN_DAT/KBD_DAT/WAND_RTS/OCIA_CLK_O	Analog	In/Out	1	RS-232 RTS/485 Differential Neg/Synapse DATA/Keyboard DATA/Wand RTS/OCIA clk out
DOWNLOAD*	Digital	Out	1	Download flag

Pin Name	Dig/Ana	In/Out	No. Pin	Description
RXD	Analog	In	1	RS-232 RXD signal
CTS/OCIA_SDATA	Analog	In	1	RS-232 CTS/Keyboard data
TRM_CLK	Analog	In/Out	1	Terminal Clock
TRM_DAT/WAND_CTS/OCIA_RDATA	Analog	In/Out	1	Terminal DATA/Wand CTS/OCIA RDATA
USB_DET/SYNC_CLK	Analog	In/Out	1	Synapse Clock
CLK_OUT	Digital	Out	1	Programmable Clock generator
DMA_REQ*	Digital	Out	1	DMA request
DMA_ACK	Digital	In	1	DMA acknowledged
IRQ*	Digital	Out	1	Interrupt Request
CMD_MODE	Digital	In	1	Command mode flag
STATUS_LED	Analog	Out	1	Status LED drive
TXD_BY	Digital	In	1	RS-232 TXD Bypass
RXD_BY	Digital	Out	1	RS-232 RXD Bypass

Total Pin 52

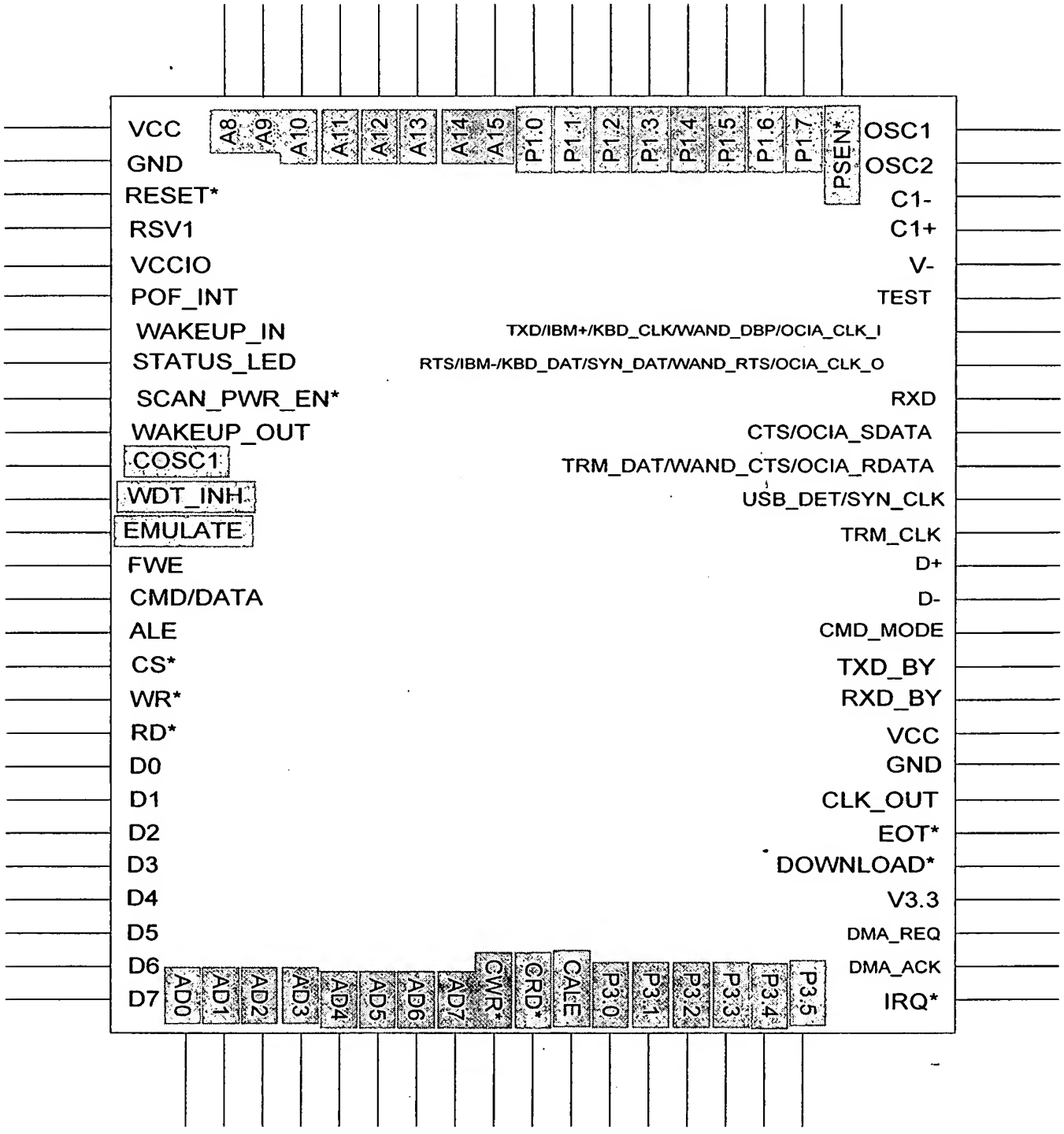


Figure 3. Chip Outline of Special Bond out Chip

8 I/O Pin Definition for the Special Bond Out Chip

Pin Name	Dig/Ana	In/Out	No. Pin	Description
VCC	Power		2	Nominal +5V
GND	Power		2	Ground
C1+			1	Positive side of voltage inversion capacitor
C1-			1	Negative side of voltage inversion capacitor
V-			1	-5V output out of charge pump
V3.3	Power	Out	1	Regulated 3.3V out
WAKEUP_OUT	Digital	Out	1	
TEST	Digital	In	1	Dedicated test pin
~~Spares~~RSV1	Digital	In/Out	1	Spare PPIA output for future use
VCCIO	Power	In	1	Digital I/O voltage
POF_INT	Digital	Out	1	USB Pulse of Frame signal
ALE	Digital	In	1	Address Latch Enable used on multiplex address/data mode
WAKEUP_IN	Digital	In	1	External wakeup input
OSC1-2	Passive		2	Crystal inputs or Resonator inputs
D0-7	Digital	In/Out	8	8-bit data bus
RD*	Digital	In	1	Read Strobe
WR*	Digital	In	1	Write Strobe
FWE	Digital	In	1	Flash Write Enable -
CMD/DATA	Digital	In	1	CMD (Address)/Data signal used in non-multiplex mode~~CMD(address) or DATA~~
CS*	Digital	In	1	Chip Select
SCAN_PWR_EN*	Digital	Out	1	Scanner power enable
RESET*	Digital	In	1	Master Reset
EOT*	Digital	Out	1	End of DMA transfer
D+	Analog	In/Out	1	USB Differential Positive out
D-	Analog	In/Out	1	USB Differential negative out
TXD/IBM+/KBD_CLK/WAND_DBP/OCIA_CLK_I	Analog	In/Out	1	RS-232 TXD/485 Differential Pos/Keyboard clock/Wand DBP/OCIA clock in
RTS/IBM-/SYN_DAT/KBD_DAT/W	Analog	In/Out	1	RS-232 RTS/485 Differential Neg/Synapse DATA/Keyboard DATA/Wand RTS/OCIA clk out

Pin Name	Dig/Ana	In/Out	No. Pin	Description
AND_RTS/OCIA_CLK_O				
DOWNLOAD*	Digital	Out	1	Download flag
RXD	Analog	In	1	RS-232 RXD
CTS/OCIA_SDATA	Analog	In	1	RS-232 CTS/Keyboard data
TRM_CLK	Analog	In/Out	1	Terminal Clock
TRM_DAT/WAND_CTS/ OCIA_RDATA	Analog	In/Out	1	Terminal DATA/Wand CTS/OCIA RDATA
USB_DET/SYNC_CLK	Analog	In/Out	1	Synapse Clock
CLK_OUT	Digital	Out	1	Programmable Clock generator
DMA_REQ*	Digital	Out	1	DMA request
DMA_ACK	Digital	In	1	DMA acknowledged
IRQ*	Digital	Out	1	Interrupt Request
CMD_MODE	Digital	In	1	Command mode flag
STATUS_LED	Analog	Out	1	LED drive transistor
TXD_BY	Digital	In	1	RS-232 TXD Bypass
RXD_BY	Digital	Out	1	RS-232 RXD Bypass
AD7-0	Digital	In/Out	8	8051 Address/Data bus
A15-8	Digital	In/Out	8	8051 Address bus
CWR*	Digital	In/Out	1	8051 Write Strobe
CRD*	Digital	In/Out	1	8051 Read Strobe
CALE	Digital	In/Out	1	8051 Address Latch Enable
P3.0-5	Digital	In/Out	6	8051 Port 3
P1.0-7	Digital	In/Out	8	8051 Port 1
PSEN*	Digital	In/Out	1	8051 PSEN
COSC1	Digital	Out	1	8051 OSC1
EMULATE	Digital	In	1	8051 Emulate enable
WDT_INH	Digital	In	1	WDT Inhibit control

Total Pin 88

9 The DC Specification

Electrical Specifications

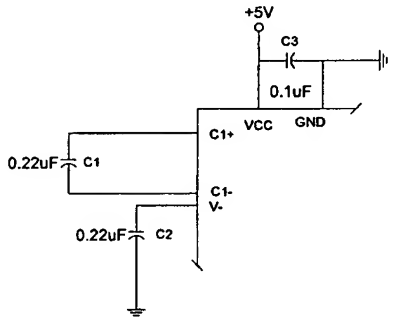
Parameter	Min	Max	Unit	Condition
Supply Current (Normal Mode)		TBD	mA	VCC = 5.25V
Supply Current (Power down Mode)		1 max	mA	VCC = 5.25V with –5V charge pump on
Supply Current Total (Suspend Mode)		~~500~~ 350 max	uA	VCC, VCCIO = 5.25V with –5V charge pump off
Supply Voltage, VCC	4.75	~~4.75~~ 5.25	V	
Supply Voltage, VCCIO	3	5.25	V	VCC = 4.75 - 5.25 V
Supply Current, VCCIO		TBD	uA	VCC, VCCIO = 5.25 V
Maximum Input Voltage Range	-5	5.7	V	For bipolar I/O pins
	-0.7	5.7	V	For uni-polar I/O pins
Internal Resistors		+/-30	%	At full temperature range

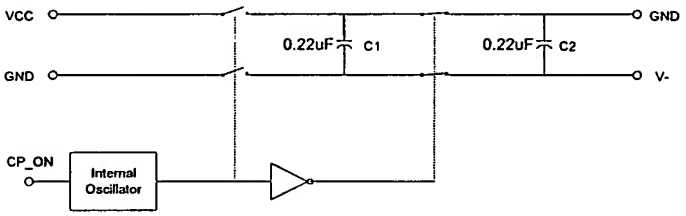
10 PLL Clock Generator

The PLL is used to multiply (X4) the input crystal or resonant frequency (12MHz) to the required 48MHz clock for the USB core. The clock oscillator shall be made so that either a low-cost crystal or a resonator can be used in application. The start-time for the PLL shall be less than 10 ms as specified in the USB specification. There shall be several clock outputs from this block, which are 48MHz, 24MHz, 1.84615MHz (24MHz divided by 13), 300KHz and clock output for external applications. The PLL on/off control shall be provided so that the PLL can be turned off via the embedded micro. This PLL_ON_OFF signal is an active low signal, which will keep the PLL oscillator on while it is low. The DPLL of USB SIE uses the 48MHz clock, whereas the CPU uses the 24MHz and 300KHz is used by the WDT.

11 Charge Pump

The charge pump is used to convert +5V to –5V for the RS-232 transceiver. It is desirable that the charge pump can be shut-off during USB suspend mode. This charge pump will run on a separate oscillator other than the PLL described above. An on/off control is required to turn this charge pump off during the USB suspend. The CP_ON control is an active high signal, which will be turning the charge pump on after power on reset. This CP_ON will be controlled via the internal 8051 processor. It is required to keep this charge pump on during USB mode due to the internal circuit switching speed requirement.





CP_ON: Charge pump on when it is '1'

Charge pump off when it is '0'

Electrical Specifications

Parameter	Typical	Unit	Condition
Internal Oscillator	120K	Hz	
V- Voltage	4.2	V	Total current = 5mA, VCC=5.0V

12 USB SIE

The USB specification shall comply fully with the USB Specification Rev. 1.1. It will only be configured as a full-speed (12Mbps) peripheral function.

- SIE (Seriales Interface Engine)
- Serial data transmit and receive
- DPLL receiver clock recovery
- CRC generation/checking
- NRZI encoding/decoding
- Bit stuffing/unstuffing
- Packet Identifier decode
- EOP detection
- Device Reset detection
- Suspend detection
- Stalled detection
- Error Checking
    - CRC error
    - Bit Stuff Errors
    - Sync Field Errors
    - EOP Errors
    - Token Errors
    - Data / Token PID Errors

- Data Toggle Errors
- Hand Shake Errors
- Byte Boundary Errors
- Error and Transaction Logging

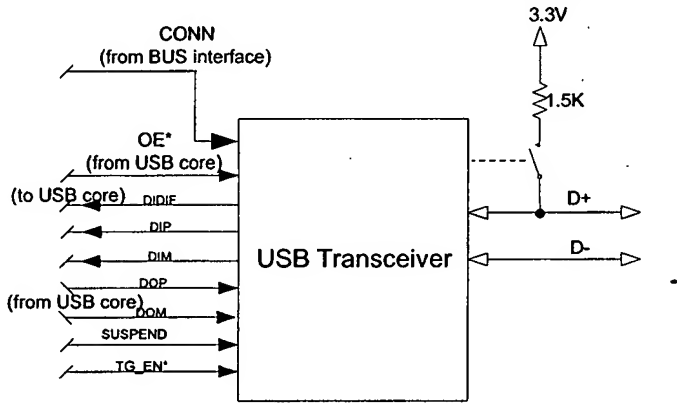
- Support Isochronous mode
  - Provide at least 1 K bytes of end point FIFO memory.

13 Processor

An 8051 or compatible processor running at 4 clocks per machine cycle or faster shall be used. The scratch pad RAM shall be 256 bytes and the total address range shall be no less than 64K bytes. There are at least two UARTs and two timers incorporated, which includes the one used for baud rate generation. There shall be two dedicated ports (e.g. port 1 and 3) available. The CPU will be operated with a 24MHz clock. The 8051 core is a Synopsys core (DW8051) that is similar to the Dallas 80C320.

14 USB Transceiver

The USB transceiver is the physical layer of USB. Only the full-speed mode is required in this transceiver design. Thus a 1.5K resistor is connected between 3.3V supply and D+ via a switch to allow connect/disconnect via the control of the 8051 processor. There are total of seven signals connected to/from the USB core. The DIDIF is the single ended differential output and the DIP, DIM, DOP, DOM is differential input and output signals from the USB SIE. The CONN signal is used to engage the pull-up



resistor whenever the USB connection is required. The TG_EN* (*active low*) signal is used to turn on the internal Transmission Gate to allow the USB output once the USB connection is established. The USB core will only establish its connection with remote host if and only if valid SETUP packet is received. The CONN signal is controlled through the 8051, where as the TG_EN* is generated by the digital hardware. It is noted that the enabling of pull-up resistors on TRM_CLK and TRM_DAT will automatically negate the TG_EN* regardless whether the USB connection is still active. The I/O truth table and its electrical specifications are asdetailed in the following table.

SUSPEND	CONN (Note 1)	OE*	DIDIF	DOP	DOM	DIP	DIM	D+	D-	

0	1	1	X	X	X	0	0	D+,(D-)<0.3V, Pull-up Resistor is enabled		Receive
0	1	1	0	X	X	0	1	D->(D+)+0.2V, Pull-up Resistor is enabled		
0	1	1	1	X	X	1	0	D+>(D-)+0.2V, Pull-up Resistor is enabled		
0	1	1	X	X	X	1	1	D-,(D+)>2.7V, Pull-up Resistor is enabled		
0	1	0	X	0	0	0	0	0	0	Transmit
0	1	0	0	0	1	0	1	0	1	
0	1	0	1	1	0	1	0	1	0	
0	1	0	X	1	1	1	1	1	1	
1	1	1 (Note 2)	1	X	X	1	0	Pull-up Resistor is Enabled; D+,D- in Input Mode		Suspend
X	0	1 (Note 2)	X	X	X	X	X	Pull-up Resistor is Opened; D+,D- in Hi-Z mode (same as Input Mode)		Transceiver is Disabled

Note 1 – The CONN going low will mean the USB D+ and D- signals will not be used, such as in the non-USB I/O modes. The CONN signal will control when the D+ and D- drivers are turned off. Whenever the CONN signal is low, the D+ and D- pins will be in high impedance state and the Differential Receiver will be turned off (zero current state).

Note 2 – In either the Suspend Mode or non-USB mode the Transceiver shall automatically be switched to the Input Mode.

Electrical Specifications

Parameter	Typical	Unit	Condition
Logic Input Threshold Low	0.8 max	V	
Logic Input Threshold High	2.4 min	V	
Logic Output High	4.6 min	V	VCC = 5V

Parameter	Typical	Unit	Condition
Logic Output Low	0.4 max	V	I = 1mA
Transceiver Output Hi Voltage	2.8 - 3.6	V	Rload = 15K
Transceiver Output Lo Voltage	0.3 max	V	Rload = 15K
Transceiver Capacitance	20	PF	Pin to GND
Transceiver Diff. Common Mode	0.8 - 2.5	V	
Transceiver Diff. Input Sensitivity	0.2	V	
Transceiver Input Hysteresis	200	mV	
Transceiver Output Risetime	4-20	ns	Cload = 50pf
Transceiver Output Falltime	4-20	ns	Cload = 50pf
Risetime/Falltime Matching	+/-10%		
Transceiver Output Crossover	1.3 - 2.0	V	
The Pull-up resistor	1.1K-1.9K	Ohm	
Analog-switch Rds ON	75 max	Ohm	
Analog-switch turn-on time	200 max	ns	
Analog-switch turn-off time	200 max	ns	
Switch feed-thru capacitance	0.5max	PF	
Transceiver Input Voltage	±5	V	

15 Bus Interface

The parallel bus interface is used to communicate with the embedded micro as well as with the clock output control. The parallel bus input/output is similar to what is illustrated in the Philips Semiconductor PDIUSBD12 datasheet.

The following specification applies to all Bus Interface logic signals, which include D0-7, WR*, RD*, CS*, ALE, A0, IRQ*, DMA_REQ, DMA_ACK, CLKOUT, EOT*.

There internal pull-up to VCCIO shall be provided for both the CS* and RESET* signals, where as pull-down shall be provided for FWE signal.

Signal Name	I/O type	Description	Polarity
D0-7	IO	Bi-direction data bus	
CS*	I	Chip select	Negative
ALE	I	Address Latch Enable	
WR*	I	write strobe	Negative
RD*	I	read strobe	Negative
A0	I	Address 1=command, 0=data	

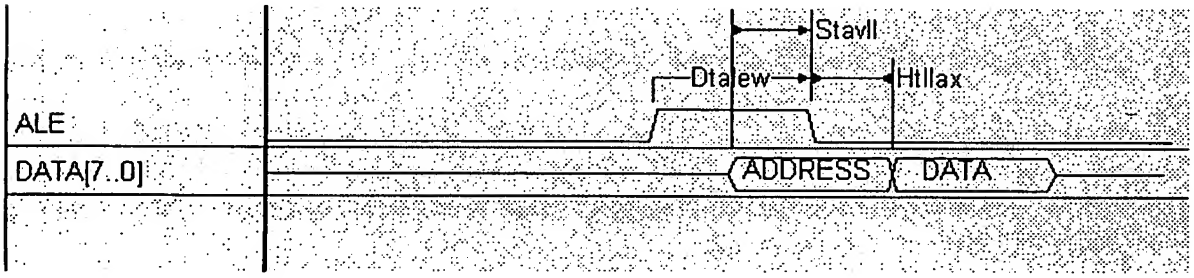
Signal Name	I/O type	Description	Polarity
DMA_REQ	O	DMA request	
DMA_ACK	I	DMA acknowledge	
EOT*	I	End Of Transfer	Negative
FWE	I	Flash Write Enable	
IRQ*	O	Interrupt Request	Negative

The Bus Interface I/O will be either 3.3V or 5V depends on the supply voltage applied to the VCCIO and its electrical specification is as the following:

Electrical Specifications

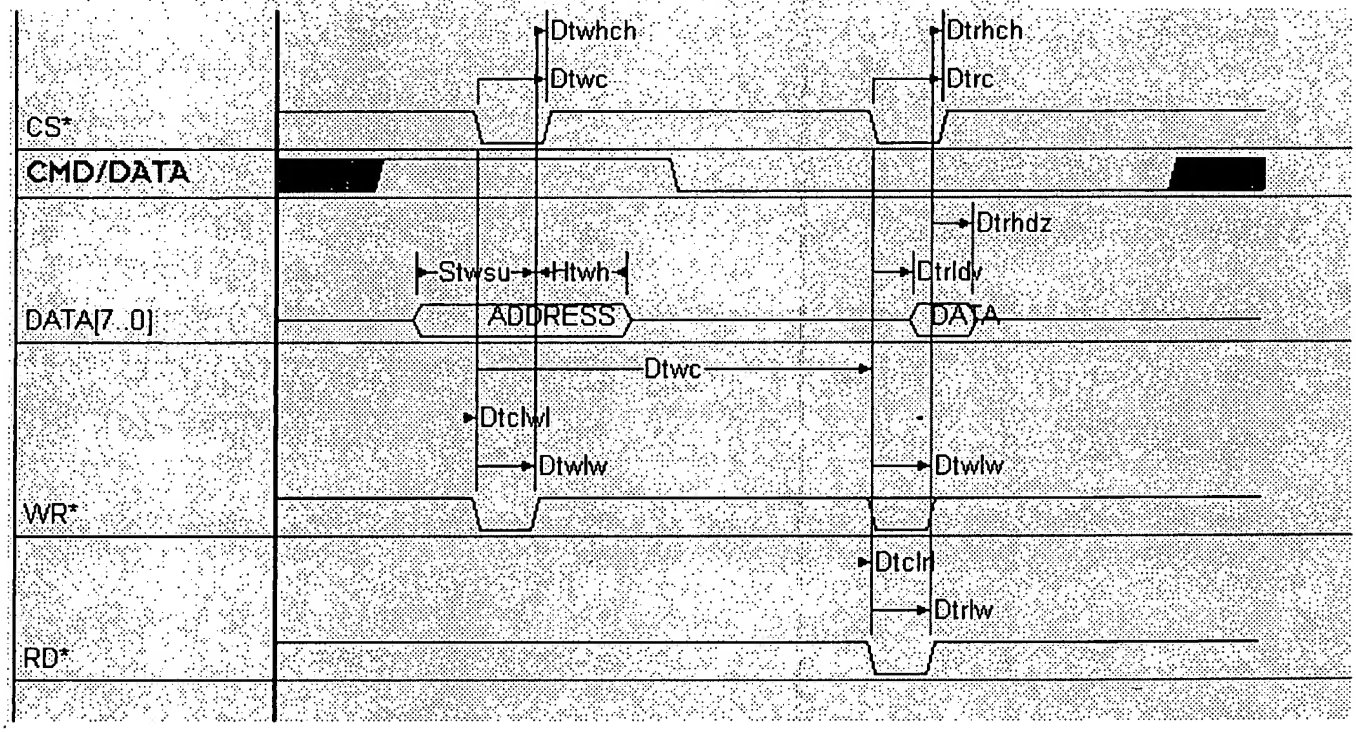
Parameter	Typical	Unit	Condition
VCCIO Voltage range	3.0 – 5.2	V	
Logic input voltage	0 - 5.5	V	
Logic Input Threshold Low	0.8 max	V	
Logic Input Threshold High	2.4 min, 3 max	V	
Logic Output High	VCCIO-0.1 min	V	I = 100uA
	VCCIO-1 min	V	I = 4mA
Logic Output Low	0.4 max	V	I = 4mA
Output Short Circuit Current	+/-25	mA	
Output Disable leakage Current	+/-10	uA	Vout = VCC or 0V
Output Rise Time	4-20	ns	Cload = 50PF
Output Fall Time	4-20	ns	Cload = 50PF
Pull-up Current	10	uA	Vin = 0V and VCCIO = 5V
Pull-down Current	10	uA	Vin = 5V and VCCIO = 5V

Using the ALE signal, the Address and Data can be multiplexed through DATA[7..0] in a same bus cycle. The actual bus cycle with ALE is depicted as the following.



name	min	max	margin	comment
Dtalew	20			width of ALE high
Stavll	10			address valid to ALE low
Hale	5			ALE low to address transition

name	min	max	comment
Dtalew	20		width of ALE high
Stavll	10		address valid to ALE low
Hale	5		ALE low hold time



In the non-ALE bus sequence, the address and data are clocked in separate bus cycles. The read bus sequence is depicted above.

And the timing constraints are as follows:

name	min	max	comment
Dtwlw	30		WR* low pulse width
Dtclwl	0		CS* low to WR* low
Stwsu	10		write data setup time
Dtwc	200		write cycle time
Htwh	10		write data hold time
Dtwhch	5		WR* high to CS* high
Dtrlw	160	5000	read pulse width
Dtrc	200	5000	read cycle time
Dtrhch	5		RD* high to CS* high
Dtclrl	0		CS* low to RD* low
Dtrldv		20	RD* low to data Valid
Dtrhdz		20	RD* high to data hi-z

name	min	max	margin	comment
Dtwlw	30		na (delay)	WR* low pulse width
Dtclwl	0		na (delay)	CS* low to WR* low
Stwsu	10		50	write data setup time
Dtwc	200		na (delay)	write cycle time
Htwh	10		36	write data hold time
Dtwhch	5		na (delay)	WR* high to CS* high
Dtrlw	160		na (delay)	read pulse width
Dtrc	200		na (delay)	read cycle time
Dtrhch	5		na (delay)	RD* high to CS* high
Dtclrl	0		na (delay)	CS* low to RD* low
Dtrldv		20	na (delay)	RD* low to data Valid
Dtrhdz		20	na (delay)	RD* high to data hi-z

The memory map is listed inas the following table:

FWE=0		FWE=1	
Address	Register	Address	Register
00H	Mailbox 0	00H - 7FH	FLASH DATA
01H	Mailbox 1	80H	Flash Page
02H	Mailbox 2	81H	Flash Status
03H	Mailbox 3	82H	Flash Error

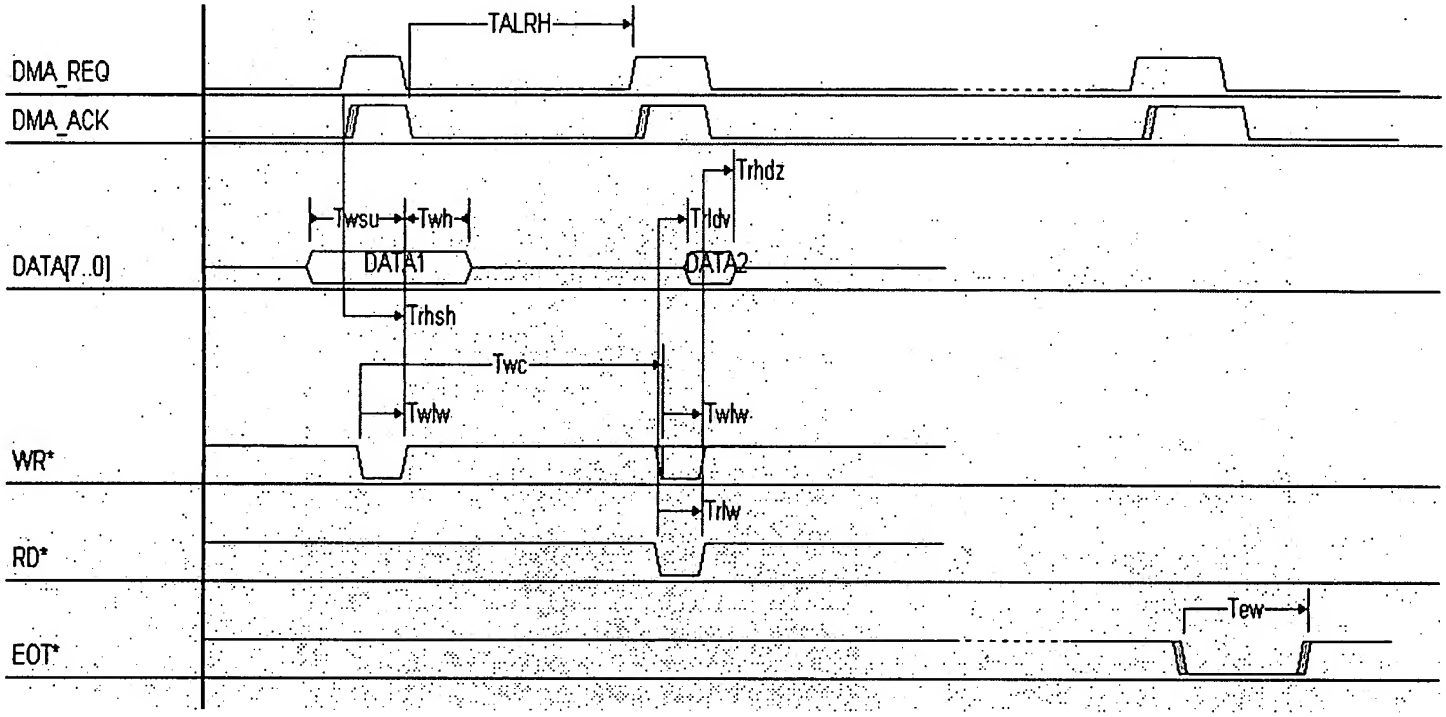
04H	Mailbox 4
05H	Mailbox 5
06H	Mailbox 6
07H	Mailbox 7
08H	Interrupt Status
09H	Interrupt Mask
0AH	Status
0BH	CLK_OUT
0CH	CLR MB INT
0DH	CLR RTS INT
0EH	Decode Pwr OVRIDE
0FH	PWR Status
10H-FFH	reserved

83H	Flash Erase Mode
84H	Flash Erase
85H - FFH	reserved

16 DMA Controller

The purpose of this DMA controller is to provide a high-speed data transfer channel between the USB FIFO and the external processor. Since DMA controllers allow the data to flow directly in or out of the processor RAM, it eliminates the overhead incurred by the mailbox data transfer described in the previous section. This is essential for those applications that require Isochronous USB mode for data transfers, such as video applications. Upon data transfer, the DMA controller will handshake with the external DMA controller via its dedicated DMA_REQ and DMA_ACK signals. In order to simplify this DMA implementation, only the single cycle mode needs to be supported in this device. The DMA controller is controlled via the embedded micro only.

The timing diagram for the DMA is as following.


TALRH
DMA_REQ
DMA_ACK
Trhdz
Twsu
Twh
Trldv
DATA[7..0]
DATA1
DATA2
Trhsh
Twc
Twlw
Twlw
WR*
Trlw
RD*
Tew
EOT*

name	min	max	comment
Trlw	30		read pulse width
Trldv		20	RD* low to data Valid
Trhdz		20	RD* high to data hi-z
Trhsh	100		Time Req High to Strobes High
Twc	200		write cycle time
TALRH	150		time from ack low to req high
Twlw	30		WR* low pulse width
Tew	83	83	time EOT pulse width

name	min	max	margin	comment
Trlw	30		na (delay)	read pulse width
Trldv		20	na (delay)	RD* low to data Valid
Trhdz		20	na (delay)	RD* high to data hi-z
Trhsh	100		na (delay)	Time Req High to Strobes High
Twc	200		na (delay)	write cycle time
TALRH	150		na (delay)	time from ack low to req high
Twlw	30		na (delay)	WR* low pulse width
Tew	83	83	na (delay)	time EOT pulse width

The following registers are used to set up the DMA controller. The address register is a 4-bit register with number 0 – 15 indicating the FIFO for end point 0 to 15. The count registers are 16 bit wide. The control register is used to commence the DMA transfer. Please be aware that the following registers are accessible only via the 8051 micro.

DMA ADDRESS REGISTER (R/W) ADDR: 9418h

D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0

DMA COUNT REGISTER MSB (R/W) ADDR: 9417h

D7	D6	D5	D4	D3	D2	D1	D0
						D19	D08

The D1 and D0 contain the two upper bit of the ten bit of the DMA count.

DMA COUNT REGISTER LSB (R/W) ADDR: 9416h

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

DMA CONTROL REGISTER (R/W) ADDR: 9419h

D7	D6	D5	D4	D3	D2	D1	D0
				INT EN	DMA DIR		DMA EN

DMA EN:	DMA enable	1: Start;	0: Stop (reset) - self clearing
DMA DIR:	DMA direction	1: DMA write;	0: DMA read (out of RAM)
INT EN:	DMA INT enable	1: ENABLE;	0: DISABLE (reset)

CLEAR DMA INTERRUPT REGISTER (W) ADDR: 941Fh

D7	D6	D5	D4	D3	D2	D1	D0

Write to this register with any data will clear the DMA interrupt.

17 Clock Generator

The clock generator shall be provided so that clock frequencies of 6, 12, 24 MHz can be programmed as output on CLKOUT. This clock output can be used as a clock source to the external micro-controller in a typical decoder application. **The clock frequency selection is performed via the bus interface.**

The electrical specification of CLKOUT is as follows:

Electrical Specifications

Parameter	Typical	Unit	Condition
*Duty Cycle	49-51	%	
Logic Output High	VCCIO-0.1 min	V	I = 100uA
	VCCIO-1 min	V	I = 4mA
Logic Output Low	0.4 max	V	I = 4mA
Output Short Circuit Current	+/-25	mA	
Output Disable leakage Current	+/-10	uA	Vout = VCC or 0V
Output Rise Time	4-20	nS	Cload = 50PF
Output Fall Time	4-20	nS	Cload = 50PF
Note: * this parameter is for the output rise/fall time symmetry.			

CLK_OUT REGISTER (R/W) ADDR: 0x0B

D7	D6	D5	D4	D3	D2	D1	D0
CLK ENA						S1	S0

CLK ENA: CLK_OUT enable 1: ENABLE (reset); 0: DISABLE

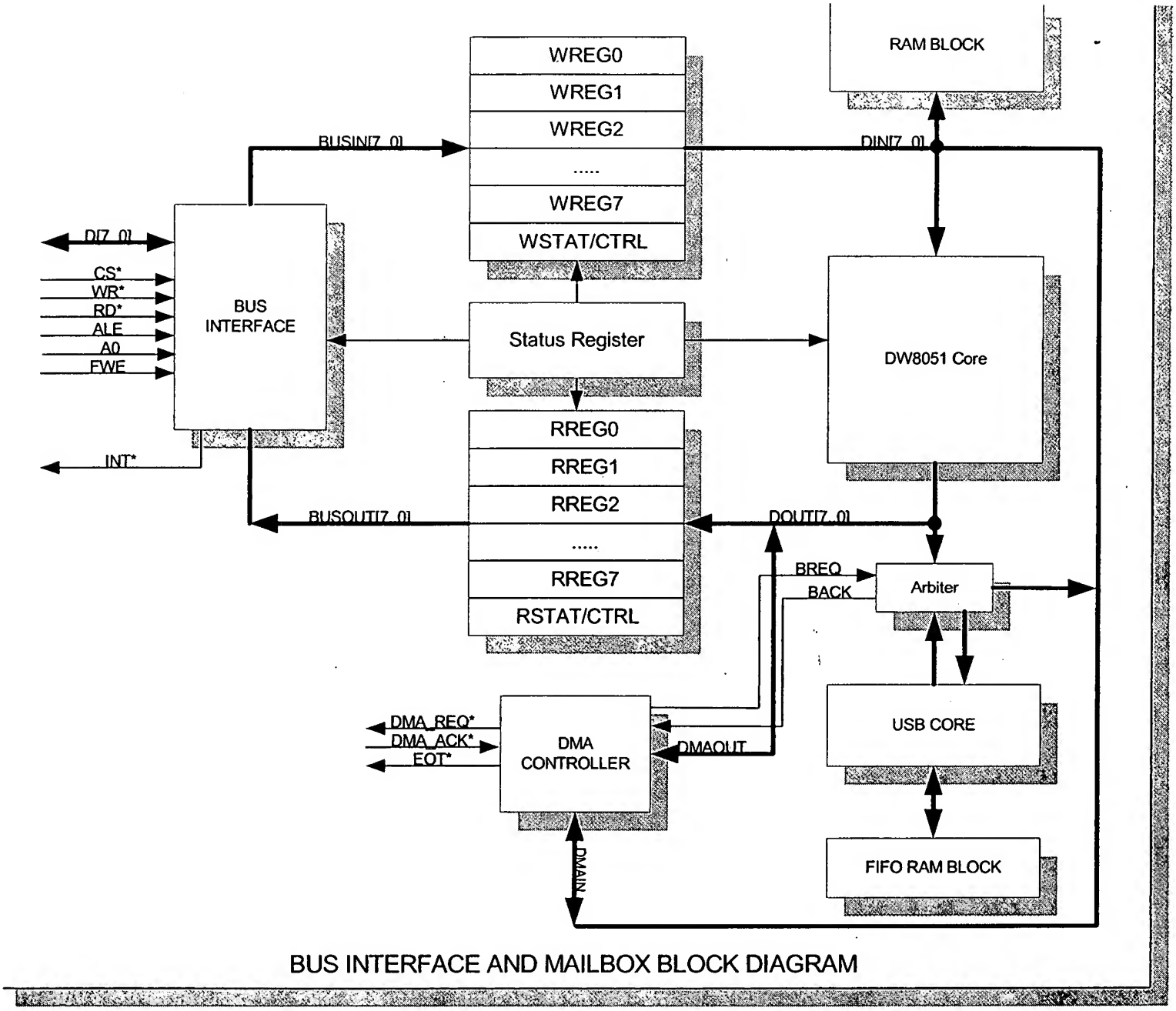
S1 – S0: 0: 6MHz(reset); 1: 12MHz; 2: 24MHz

The (reset) next to the state indicates the default setting after RESET.

18 Mailbox I/O Block

The diagram labeled "BUS INTERFACE AND MAILBOX DIAGRAM" depicts the basic architecture of the mailbox I/O block. The mailbox is designed to facilitate the command and data transfer between the external processor and the embedded 8051 micro. Although the read and write to the mail boxes are sharing the same address, there are physically two separate sets of eight registers dedicated to the input and the output mail boxes as noted WREG(0-7) and RREG(0-7) in the following diagram. Interrupts shall be generated upon the writing and the reading of register 7. The writing of WREG7 will cause the interrupt to the 8051, where as the reading of WREG 7 via 8051 will cause interrupt being generated to the external processor. Both the buffer full and empty interrupt shall be made programmable via processor control as described later in this section. The status register shall be made available to both sides. In addition, there shall be a semaphore available for each side to signal its readiness. This shall be done via the standard interface without added extra I/O pins. They are called the MB_RTS and MB_CTS hereafter to avoid any confusion. The 8051 processor owns the MB_RTS, where as the MB_CTS does the external scanner processor control. There are two registers set aside to clear the Mailbox interrupt and CTS interrupts.

Since the power to the external scanner is controlled via the 8051, the power status of this chip can be monitored by the external micro via the power status register. This power status register contains not only the power status of the scanner but also the PLL on/off status of this chip. There will be another register to allow the external micro to prohibit the 8051 from removing its power. The detail description of the power state and control registers will be in the Wake Up and Power Control section of this document.



BUS INTERFACE AND MAILBOX BLOCK DIAGRAM

MAILBOX INTERRUPT CONTROL (8051) REGISTER (R/W) ADDR: 9409h

D7	D6	D5	D4	D3	D2	D1	D0
WREG[1] FULL	RREG[1] EMTY	D5	D4	D3	D2	D1	D0

WREG FULL: interrupt on WREG filled by ext. proc. 1: enabled 0: disabled;

RREG EMPTY: interrupt on RREG emptied by ext. proc. 1: enabled 0: disabled;

MAILBOX INTERRUPT STATUS (8051) REGISTER (R) ADDR: 940Ah

D7	D6	D5	D4	D3	D2	D1	D0
WREG[1] FULL	RREG[1] EMTY	D5	D4	D3	D2	D1	D0

WREG FULL: flag signals the WREG full event 1: buffer filled 0: nothing;
Reading the Mailbox 7 clears the interrupt.
RREG EMPTY: flag signals the RREG empty event 1: buffer emptied 0: nothing;
Writes to CLEAR MB EMPTY INTERRUPT REG (941Ch) will clear the interrupt.

CLEAR MB EMPTY INTERRUPT REGISTER (W) ADDR: 941Ch

D7	D6	D5	D4	D3	D2	D1	D0

Writes to this register will clear the RREG EMTY interrupt.

MAILBOX INTERRUPT CONTROL (EXTERNAL) REGISTER (R/W) ADDR: 09H

D7	D6	D5	D4	D3	D2	D1	D0
RREG[1] FULL	WREG[1] EMTY	RTS EVENT				PULSE INT	INT POL

RREG FULL: interrupt on RREG filled by MIA's 8051 1: enabled 0: disabled;
WREG EMPTY: interrupt on WREG emptied by MIA's 8051 1: enabled 0: disabled;
RTS EVENT: MB_RTS event interrupt 1: enabled 0: disabled;
PLUSE INT: PULSE interrupt or LEVEL interrupt 1: PULSE 0: LEVEL; 160ns Pulse
INT POL: interrupt signal polarity 1: active high 0: active low;

MAILBOX INTERRUPT STATUS (EXTERNAL) REGISTER (R) ADDR: 08H

D7	D6	D5	D4	D3	D2	D1	D0

RREG[1] FULL	WREG[1] EMTY	RTS INT					

RREG FULL: flag signals the RREG full event 1: buffer filled 0: nothing;

WREG EMPTY: flag signals the WREG empty event 1: buffer emptied 0: nothing;

RTS INT: flag signals the MB_RTS event interrupt 1: Event_occurred 0: nothing;

MAILBOX STATUS (EXTERNAL/INTERNAL) REGISTER (R/W) ADDR: 0AH/9408h

D7	D6	D5	D4	D3	D2	D1	D0
RREG[1] FL/RD	WREG[1] FL/RD	RTS[2] FLAG	CTS[3] FLAG				

RREG FL/RD : flag set to '1' when the RREG is filled and clear to '0' when the RREG is emptied;

WREG FL/RD: flag set to '1' when the WREG is filled and clear to '0' when the WREG is emptied;

RTS FLAG: RTS flag is set or reset by the 8051 1: set 0: reset;

CTS FLAG: CTS flag is set or reset by the external processor 1: set 0: reset;

MAILBOX (EXTERNAL/INTERNAL) REGISTER 0-7 (W/R) ADDR: 00-07H/9400-9407h

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

Notes:

[1] Both the FULL and EMPTY interrupts or status are modified upon the writing and reading of the 7th register of either WREG or RREG.

[2] Only the RTS FLAG can be written by the MIA's 8051 process with a '1' or '0'. Writing to other bits of this register has no effects on them.

[3] Only the CTS FLAG can be written by the external process with a '1' or '0'. Writing to other bits of this register has no effects on them.

Although the reading and writing of the mailbox are done through the same addresses, **there are two physical banks of mailbox registers**. The reading and writing are always pertaining to its perspective incoming and outgoing mail registers. For example, the internal 8051 processor can only write to the RREG0-7 and read from the WREG0-7, where as the external processor only writes to the WREG0-7 and reads from the RREG0-7.

19 FLASH ROM/Static RAM

The total amount of program space in the FLASH ROM shall be 32Kilo-bytes. The FLASH block shall be partitioned into 128-byte erasable sectors. The device shall provide required FLASH programming voltages so that In-System-Programmability is available without additional supply voltages other than the prime voltage (+5VDC). The FLASH shall guarantee at least ten thousand (10,000) reprogramming cycles.

There should be 2K bytes of Static RAM embedded in this device in addition to the 256-byte scratch pad for the 8051. Both ROM and RAM shall be setup for byte-wide (8-bit) access. The read access time for FLASH ROM shall be no worse than 80ns and no worse than 20ns for SRAM read/write accesses.

20 FLASH ROM Programming

The programming of this embedded FLASH will be designed without micro intervention, which would otherwise require additional RAM to facilitate the FLASH load. The underlying FLASH programming method reflects a generic FLASH device programming. Upon detecting the FLASH WRITE (via FWE signal), the device will enter its FLASH memory mode. Meanwhile, the embedded micro will relinquish control of all buses and hold itself in reset state. The local controller can then access the embedded FLASH blocks as if it is a passive memory device. In order for the local controller to communicate with an external host during FLASH programming, the TXD and RXD will be bypassed to the local controller. The full 32K of FLASH block is divided into 256 of 128 byte sectors. This arrangement is to work around the limitation of using the 8-bit bus. Conjoining both the PAGE register and the offset of the seven LSB bits from the address makes up the actual address to the FLASH memory. Once the PAGE register is set, subsequent access will be made to the page locations offset by the ADDRESS latch (refer to bus interface for ADDRESS latch). It is important to remember that the following registers are only visible while Flash Write Enable (FWE) is active.

FLASH DATA REGISTER (R/W) ADDR: 0-7FH

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7-D0: the 8 bit data that gets writeten/read from the flash. The actual FLASH address is made up of the page register and the address, which are fifteen bits total.

FLASH PAGE/SECTOR REGISTER (R/W) ADDR: 80H

D7	D6	D5	D4	D3	D2	D1	D0
P7	P6	P5	P4	P3	P2	P1	P0

P7-P0: the 8-bit sector number of the FLASH memory address. Each sector contains 128 bytes. And there are total of 256 sectors.

FLASH STATUS REGISTER (R) ADDR: 81H

D7	D6	D5	D4	D3	D2	D1	D0
FAE							FM_RDY

FAE: Flash Access Error, indicates attempting to access Flash while busing programming or erasing, active high.

FM_RDY: 1: Ready 0: Busy

FLASH ERROR REGISTER (R) ADDR: 82H

D7	D6	D5	D4	D3	D2	D1	D0
SFC						UEC	UWC

SFC: Successful Flash Command, after complete erase or program command, active high.

UEC: Unsuccessful Erase Command that indicates not all bits became a '0' after erase command, active high.

UWC: Unsuccessful Write Command that indicates not all bits became a '0' after erase command, active high.

FLASH ERASE MODE REGISTER (R/W) ADDR: 83H

D7	D6	D5	D4	D3	D2	D1	D0
						M1	M0

M1-M0: 00 – invalid erase mode

01 – sector erase (128 bytes)

10 – page erase (2K bytes)

11 – block erase (32K bytes)

The page or sector address resides in the PAGE/SECTOR register.

FLASH ERASE REGISTER (W) ADDR: 84H

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1

This register is used to generate an erase strobe to the FLASH memory. The erase mode is determined by the content of the ERASE MODE register. In order to prevent inadvertent erasures, the data content

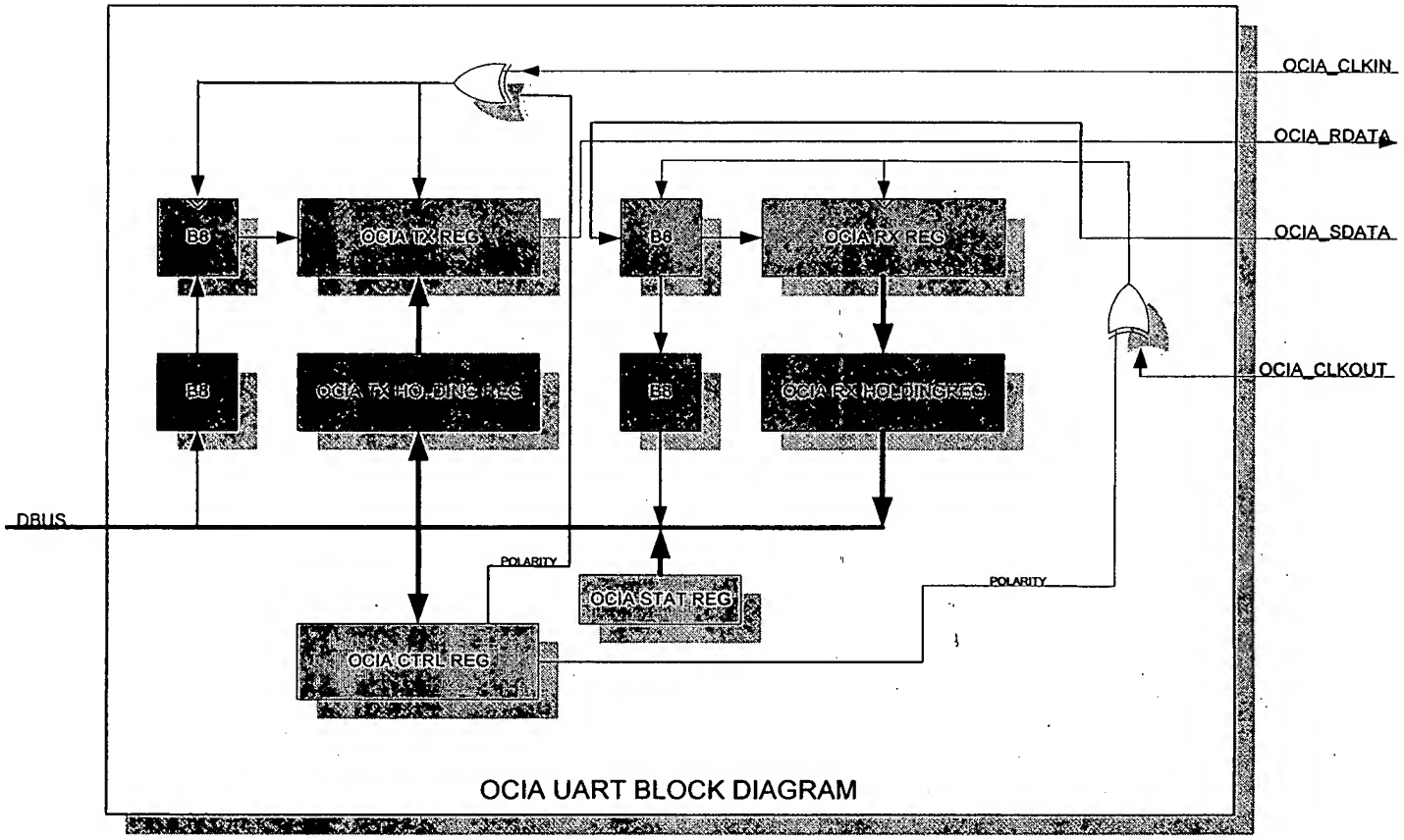
has to be 55H. Data value of other than 55H shall be writing to the same register after the Erase is finished (i.e. to issue a new erase command, write in 00H then write 55H).

21 UART

The UART shall support at the minimum the following baud rates: 110, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 187500 (only for RS-485) BPS. For the 8051 processor, Timer 2 shall be provided as baud rate generator. With a 24MHz CPU clock, timer 2 will use the 12MHz clock (8051 CPU clock divided by 2) and use it to generate the required 16x-baud rate clock for the UART. The timer 2 shall also be able to use the external (T2 input) clock input so that 115.2K and 38.4K baud can be generated using the external 1.8461MHz clock. The UART shall have parity generation functionality for both transmission and receiving as an instrument for error detection. It shall also detect parity and overrun errors.

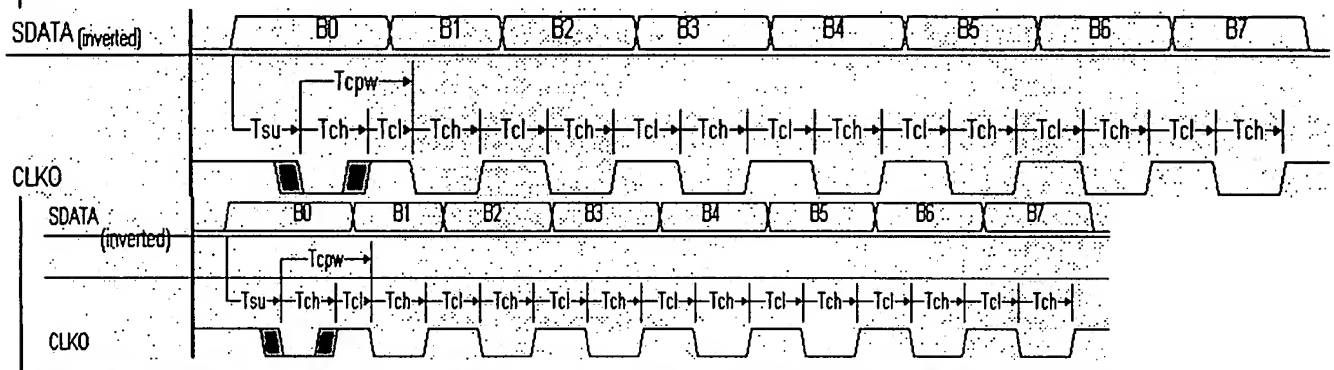
22 OCIA

The OCIA is a full duplex synchronous serial interface with dedicated clock and data for each data direction. Its clock rate is typical 300Kilo Hertz. With its full duplex implementation, the OCIA consists of three input signals and one output signal. The CLKOUT and ~~RDATA~~ SDATA pair is used to transmit data from the host into the ASIC, where as the CLKIN and ~~S~~RDATA pair is to output data to the host. Both the input and output data shall support the 8bit (S-format) as well as the 9bit (F-format) OCIA data formats. Registers such as control, status and data shall be implemented for this interface. Within the control register, programmability such as 8/9 bits data, polarity selection on both in and out clocks shall be provided. Since the transmit data stream (RDATA) will start with a ready bit first, this would extend an 8/9 bit data to 9/10 bits. The following block diagram illustrates its overall configuration. Digital filtering technique shall be implemented to eliminate noise on both the CLKI and CLKO signal lines. During it application, the OCIA_RDATA signal is normally connected to an open drain transistor, whereas the rest of the signals are outputs from CMOS receivers. Therefore, signal inversion is not required designing with this ASIC. The waveform diagram in the following pages illustrates the signal timing requirements. It should be noted that the required optical couplers are not enclosed in this ASIC. External optical couplers have to be used to complete the OCIA interface design. The RDATA output consists of an open drain transistor that can sink up to 5mA and can possibly drive an optical coupler directly. Otherwise, an external drive device, such as transistor, must be used.

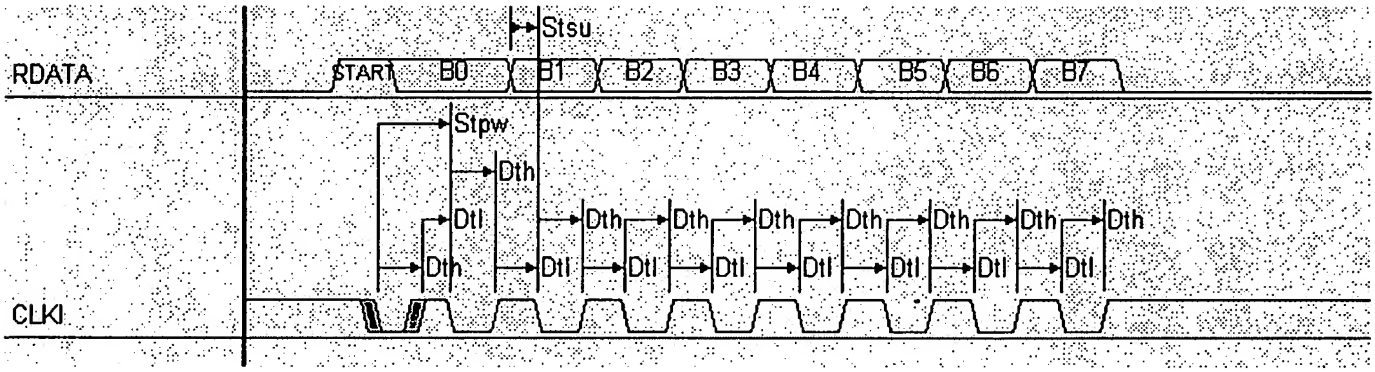


OCIA UART BLOCK DIAGRAM

The following signal waveform and timing are for both SDATA and RDATA. The SDATA is inverted out of the optical coupler.



name	min	max	margin	comment
Tch	1500		na (delay)	time clock high
Tcl	1500		na (delay)	time clock low
Tcpw	3000		na (delay)	clock pulse width
Tsu	1000		na (delay)	data setup time



name	min	max	comment
Dth	1500		pulse width clock high
Dtl	1500		pulse width clock low
Stpw	3000		clock pulse width
Stsu	1000		

name	min	max	margin	comment
Dth	1500		na (delay)	pulse width clock high
Dtl	1500		na (delay)	pulse width clock low
Stpw	3000		na (delay)	clock pulse width
Stsu	1000		0	

The simplified control and clock out control registers are defined as the following:

OCIA CONTROL REGISTER (R/W) ADDR: 9410h

D7	D6	D5	D4	D3	D2	D1	D0
CLKI POL	CLKO POL	RX INT	TX INT		SHORT /EXT	RX ENA	TX ENA

CLKI POL:	1 – clock on rising-edge	0 – clock on falling-edge (reset)
CLKO POL:	1 – clock on rising-edge	0 – clock on falling-edge (reset)
SHORT/EXT:	1 – 8 bit (reset)	0 – 9 bit extended mode
RX ENA:	1 – receive enabled	0 – receive disabled (reset)
TX ENA:	1 – transmit enabled	0 – transmit disabled (reset)
RX INT	1 – RX interrupt enabled	0 – RX interrupt disabled (reset)
TX INT:	1 – TX interrupt enabled	0 – TX interrupt disabled (reset)

Both the RX and TX interrupt will be generated as edge sensitive interrupts. In other word, the DR interrupt will only be generated upon the data received. The Transmit Buffer Empty interrupt will consequently be generated on the instance when the buffer becomes empty.

OCIA STATUS REGISTER (R) ADDR: 9411h

D7	D6	D5	D4	D3	D2	D1	D0
INT FLAG						DR	TB EMPT

INT FLAG:	1 – interrupt generated	0 – no interrupt
DR:	1 – Data received	0 – no data (reset)
TB EMPT:	1 – transmit buffer empty (reset)	0 – transmit buffer not empty

Reading this register will clear the INT FLAG bit, where as reading data receive register will clear the DR flag.

OCIA TRANSMIT DATA REGISTER LSB (R/W) ADDR: 9412h

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

OCIA TRANSMIT DATA REGISTER MSB (R/W) ADDR: 9413h

D7	D6	D5	D4	D3	D2	D1	D0
							D8

The OCIA TDR MSB is only valid on 9-bit transmission.

OCIA RECEIVE DATA REGISTER LSB (R/W) ADDR: 9414h

D7	D6	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

OCIA RECEIVE DATA REGISTER MSB (R/W) ADDR: 9415h

D7	D6	D5	D4	D3	D2	D1	D0
							D8

The OCIA RDR MSB is only valid on 9-bit transmission.

23 Programmable Interval Timer

The 16-bit tTimer0-2 should be made available the same way as of a standard 8051 processor. But during the RS-232 and RS-485 mode, the tTimer2 will be used for baud rate generation. The tTimer2 can use either half of the CPU clock (12Mhz) or the external clock input (1.8Mhz) to generate the required baud rate clock. Timer1 can be used as either a general-purpose time or as baud rate generator for debugging using serial port 1.

24 Watch Dog Timer

The watch dog timer can be used to generate either an interval interrupt or to reset the micro in the case that the micro failed to refresh the watch dog timer. Both the interrupt and CPU reset are generated upon counter overflow. The WDT is an up count only counter and it will generate interrupt or reset when the counts overflow (from FFH to 00H) occurs. There are two registers associated with this WDT, the WDT control/status register and write-only WDT register.

WDT CONTROL/STATUS REGISTER (R/W) ADDR: 940Ch

D7	D6	D5	D4	D3	D2	D1	D0
WDT	OVR	INT		RUN/STOP	S2	S1	S0

WDT: 1 – watch-dog timer mode 0 – internal timer mode (reset)

OVR: read only – overflow indicator, reset after read

INT: 1 – interrupt enable Interrupt is cleared by reading register.

RUN/STOP: 1 – Run 0 – Stop (reset)

S2-S0: clock selection

0 0 0	:	3.3 µs (reset)	300khz
0 0 1	:	13.2 µs	300k/4
0 1 0	:	52.8 µs	300k/16
0 1 1	:	211.2 µs	300k/64
1 0 0	:	1.69 ms	300k/512
1 0 1	:	13.5 ms	300k/4096
1 1 0	:	54.1 ms	300k/16384
1 1 1	:	216.2 ms	300k/65536

WDT REGISTER (W) ADDR: 940Dh

D7	D6	D5	D4	D3	D2	D1	D0
C7	C6	C5	C4	C3	C2	C1	C0

25 USB Control and Configuration

This section defines the USB to micro interface. There are numerous control and status registers that are dedicated to the USB function. Control registers shall include general control, endpoint control, address register, interrupt control and error (stall) generation. Status registers shall contain general status, error status, interrupt status and frame number register.

The definitions of the above registers are outlined in the Inventra MUSBFSFC pProduction sSpecification and uUser's gGuide. The base address of the USB block is at 9800h.

26 I/O Interrupts

The internal 8051 shall be able to handle all I/O interrupts via its standard INT pins. This should include MAILBOX, DMA, USB, OCIA, WDT, SOF, WAKEUP and CTS/RTS mailbox handshake interrupts. The required interrupt control and status registers are listed as the following:

CPU INTERRUPT MASK REGISTER (R/W) ADDR: 941Bh

D7	D6	D5	D4	D3	D2	D1	D0
MIA CTS	~~WAK UP~~	SOF INT	~~WDT INT~~	~~USB INT~~	~~OCIA INT~~	~~MAIL INT~~	~~DMA INT~~

For each interrupt mask bit, '1' means enable and '0' means disable the associated interrupt. The rest of the interrupt controls are located within the individual control register (i.e. the WDT control, DMA control registers, etc.).

CPU INTERRUPT STATUS REGISTER (R) ADDR: 941Ah

D7	D6	D5	D4	D3	D2	D1	D0
MIA CTS	WAK UP	SOF INT	WDT INT	USB INT	OCIA INT	MAIL INT	DMA INT

This register allows the 8051 to solicit the source of interrupt. This is especially for those interrupts that share the same INT pins. It is noted that reading of this register does not clear any interrupt. The MIA CTS interrupt can be cleared by writing the CTS CLEAR REGISTER (941Dh). The CLEAR SOF INTERRUTP REGISTER (941Eh) and CLEAR DMA INTERRUPT REGISTER (941Fh as described in the DMA section) are used to clear SOF and DMA interrupts. For the remaining of the interrupts, please refer to its respective section on how to clear the interrupts.

CLEAR CTS INTERRUPT REGISTER (W) ADDR: 941Dh

D7	D6	D5	D4	D3	D2	D1	D0

Write to this register with any data will clear the CTS interrupt.

CLEAR SOF INTERRUPT REGISTER (W) ADDR: 941Eh

D7	D6	D5	D4	D3	D2	D1	D0

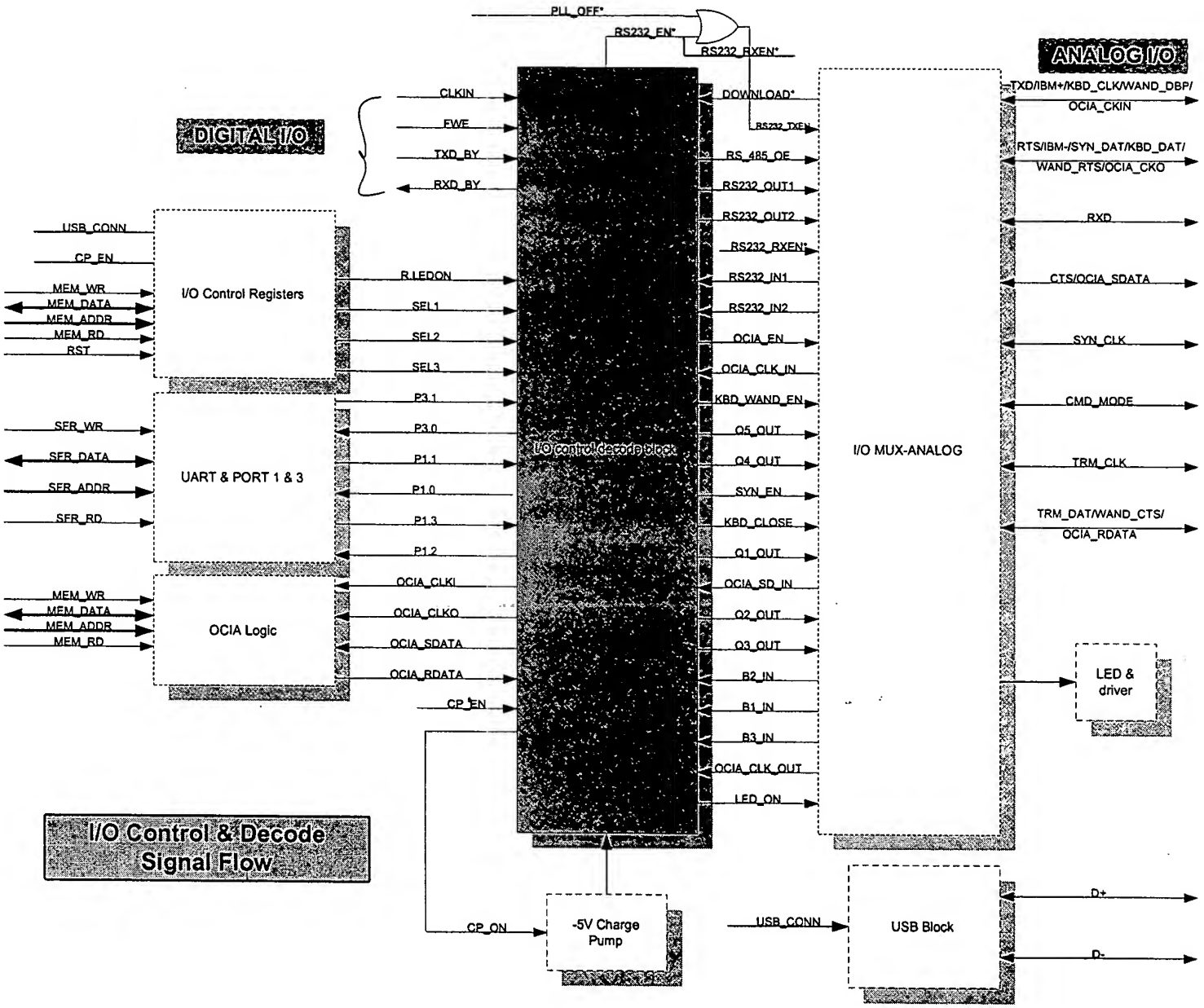
Write to this register with any data will clear the CTS interrupt.

The allocation of interrupts is:

INT0: WAKEUP, WDT, CTS
INT1: MAILBOX
INT2: OCIA, USB
INT5: SOF, DMA

27 I/O Control Logic Block

The I/O Control Logic and its related signal flow are depicted in the ~~next~~following diagram.


PLL_OFF*
RS232_EN*
RS232_RXEN*
DIGITAL I/O
CLKIN
FWE
TXD_BY
RXD_BY
USB_CONN
CP_EN
MEM_WR
MEM_DATA
MEM_ADDR
MEM_RD
RST
I/O Control Registers
R_LEDON
SEL1
SEL2
SEL3
P3.1
P3.0
P1.1
P1.0
P1.3
P1.2
SFR_WR
SFR_DATA
SFR_ADDR
SFR_RD
UART & PORT 1 & 3
OCIA_CLKI
OCIA_CLKO
OCIA_SDATA
OCIA_RDATA
MEM_WR
MEM_DATA
MEM_ADDR
MEM_RD
OCIA Logic
CP_EN
I/O control decode block
DOWNLOAD*
RS232_TXEN
RS_485_OE
RS232_OUT1
RS232_OUT2
RS232_RXEN*
RS232_IN1
RS232_IN2
OCIA_EN
OCIA_CLK_IN
KBD_WAND_EN
Q5_OUT
Q4_OUT
SYN_EN
KBD_CLOSE
Q1_OUT
OCIA_SD_IN
Q2_OUT
Q3_OUT
B2_IN
B1_IN
B3_IN
OCIA_CLK_OUT
LED_ON
I/O MUX-ANALOG
ANALOG I/O
TXD/IBM+/KBD_CLK/WAND_DBP/
OCIA_CKIN
RTS/IBM-/SYN_DAT/KBD_DAT/
WAND_RTS/OCIA_CKO
RXD
CTS/OCIA_SDATA
SYN_CLK
CMD_MODE
TRM_CLK
TRM_DAT/WAND_CTS/
OCIA_RDATA
LED &
driver
CP_ON
-5V Charge
Pump
USB_CONN
USB Block
D+
D-
I/O Control & Decode
Signal Flow

Truth table of I/O interface controls

DOWNLOAD*	F.WE	S2	S1	S0	OCIA_EN	RS_485_OE	RS_232_EN*	KBD_CLOSE	KBD_WAND_EN	SYN_EN	RS232_OUT1	RS232_OUT2	Q1_OUT	Q2_OUT	Q3_OUT	Q4_OUT	Q5_OUT	LED_ON	RXD_BY	P3.0	P3.5	P3.4	OCIA_CLKI	OCIA_CLKO	OCIA_RDATA	Comments
1	0	0	0	0	1	0	1	0	0	0	1	1	OCIA_RDATA	0	0	0	0	R.LEDON	1	1	0	0	OCIA_CLK_IN	OCIA_CLK_OUT	OCIA_SD_IN	OCIA
1	0	0	0	1	0	0	0	0	0	0	P3.1	P1.1	0	0	0	0	0	R.LEDON	1	RS232_IN1	RS23_IN2	0	0	0	0	RS-232
1	0	0	1	0	0	0	1	0	1	0	1	1	P1.1	P1.6	0	0	1	R.LEDON	1	1	B1_IN	B2_IN	0	0	0	KBD_OPEN
1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	R.LEDON	1	1	B1_IN	B2_IN	0	0	0	KBD_CLOSE
1	0	1	0	0	0	0	1	0	0	1	1	1	0	0	P1.1	P1.6	0	R.LEDON	1	1	B3_IN	OCIA_CLK_OUT	0	0	0	SYNAPSE
1	0	1	0	1	0	1	1	0	0	0	P3.1	1	0	0	0	0	0	R.LEDON	1	OCIA_CLK_IN	0	0	0	0	0	IBM_XMTR
1	0	1	1	0	0	0	1	0	0	0	P3.1	1	0	0	0	0	0	R.LEDON	1	OCIA_CLK_IN	0	0	0	0	0	IBM_RCVR
1	0	1	1	1	0	0	1	0	1	1	1	1	0	0	0	P1.6	P1.1	R.LEDON	1	1	B1_IN	0	0	0	0	WAND_EMUL
0	X	X	X	X	0	0	0	0	0	0	TXD_BY	1	0	0	0	0	0	R.LEDON	RS232_IN1	1	0	0	0	0	0	dDownload
1	1	X	X	X	0	0	1	0	0	0	1	1	0	0	0	0	0	R.LEDON	1	1	0	0	0	0	0	FLASH WRITE no download

X: don't care

28 Interface Control

The interface selection, LED on/off, USB_CONN, RES_IN and charge pump enable are controlled through this functional block. The interface control register is detailed in the following.

INTERFACE CONTROL REGISTER (R/W) ADDR: 940Bh

D7	D6	D5	D4	D3	D2	D1	D0
CP_ON	USB_Conn	LED_ON	RES_IN		SE3	SE2	SE1

CP_ON:	-5V charge pump ON	1: ON	0: OFF	reset: ON
USB_Conn:	Control the 1.5K PU RES.	1: IN	0: OUT	reset: OUT
LED_ON:	debug LED on/off ctrl	1: ON	0: OFF	reset: OFF
RES_IN:	pull-up resistors	1: IN	0: OUT	reset: OUT

SE3-SE1:

0 0 0	:	OCIA
0 0 1	:	RS-232
0 1 0	:	Keyboard Wedge - Open
0 1 1	:	Keyboard Wedge - Close
1 0 0	:	Synapse
1 0 1	:	IBM Send
1 1 0	:	IBM Receive
1 1 1	:	WAND Emulation

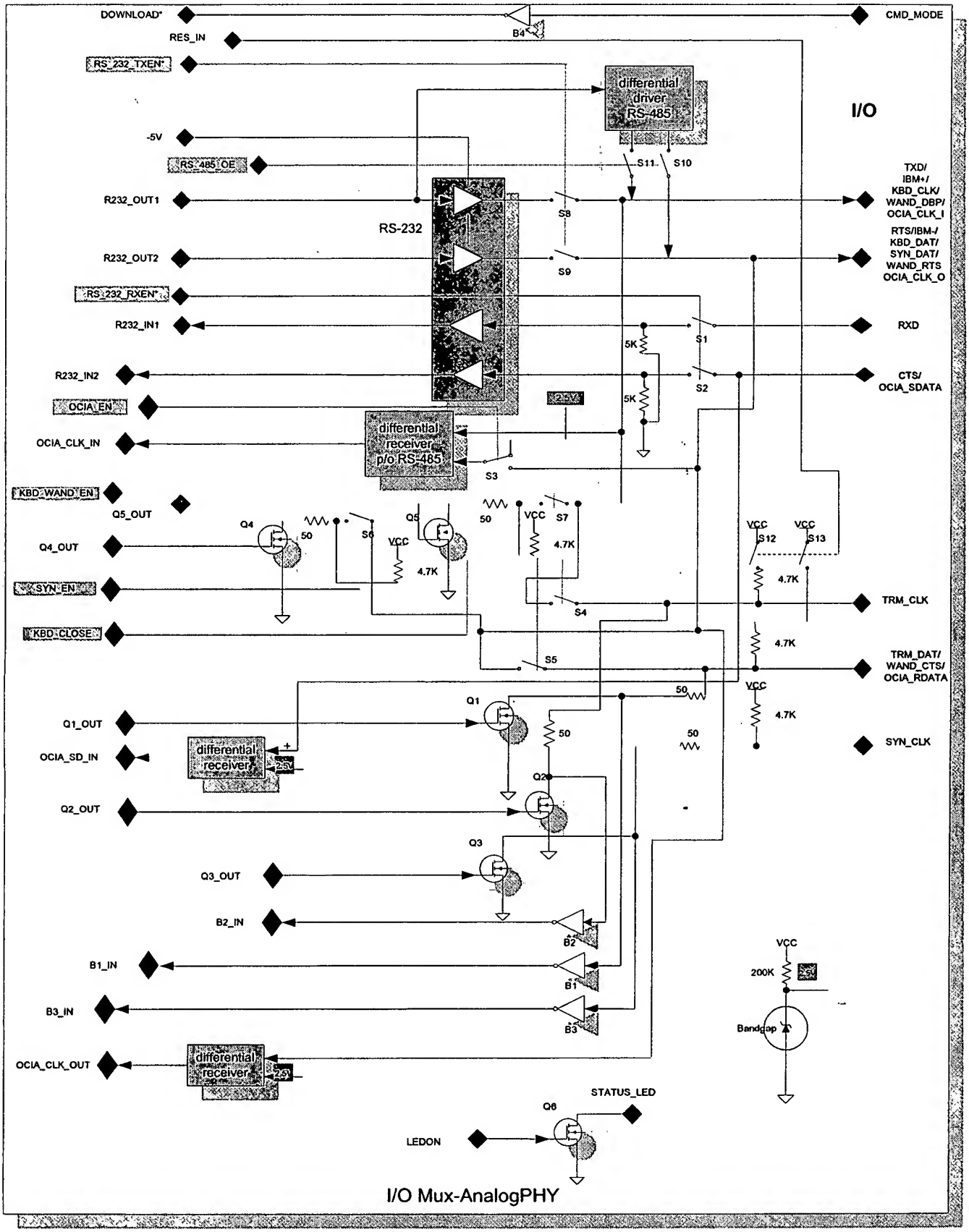
29 Interface Decode Logic

This interface decode logic is used to multiplex 8051 port pins to the appropriate I/O control signals in the analog I/O block. This block is also responsible for turning on or off appropriate analog switches upon I/O interface selection. Besides these interface selection input signals, SELx, Flash Write Enable and the download flag are all govern the outputs from this block. For example, the download enable will force the TXD and RXD of RS232 to bypass the internal processor. The overall decode truth table is listed ion the previous page.

30 I/O Mux-Analog PHY

The I/O Mux-Analog block is illustrated on the next page. This analog section includes various physical I/O circuits. There will be only one I/O interface enabled at a time. The switches were designed in order to permit multiplexing of all the different interface signals. The USB D+ and D- and TRM_CLK and TRM_DAT have their dedicated I/O pads in the chip. Ultimately, these signals may be sharing I/O connections with other I/O signals, such as RXD and CTS, due to the limited I/O pins available on a standard connector used by Symbol. Therefore, the following signals have ~~to be~~been made ±5V tolerant.

1. RXD
2. CTS /OCIA_SDATA
3. D+
4. D-
5. TRM_CLK
6. TRM_DAT/WAND_CTS/OCIA_RDATA



I/O Mux-AnalogPHY

The enable control signal to each of the above I/O switches are as following:

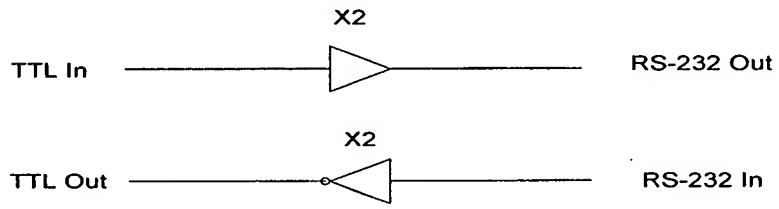
RS_485_OE:	'1' or logic high shall close S10 and S11. '0' or logic low shall open make S10 and S11 open.
RS_232_RXEN*:	'1' or logic high shall open S1 and S2. '0' or logic low shall close S1 and S2.
RS_232_TXEN*:	'1' or logic high shall open S8 and S9. '0' or logic low shall close S8 and S9.
OCIA_EN:	'1' or logic high shall switch S3 to its upper position. '0' or logic low shall switch S3 to its lower position.
KBD_WAND_EN:	'1' or logic high shall close S7. '0' or logic low shall open S7.
SYN_EN:	'1' or logic high shall close S6. '0' or logic low shall open S6.
KBD_CLOSE:	'1' or logic high shall close S4, S5. '0' or logic low shall open S4, S5.
RES_IN:	'1' or logic high shall close S12 and S13. '0' or logic low shall open S12 and S13.

The required I/O signals for each interface is:

OCIA:	OCIA_CLK_IN, OCIA_RD_IN, OCIA_CLK_OUT
RS-232:	RS232_OUT1, RS232_OUT2, RS232_IN1, RS232_IN2
KEYBOARD WEDGE:	B1_IN, B2_IN, Q1_OUT, Q2_OUT, Q5_OUT
SYNAPSE:	OCIA_CLK_OUT, B3_IN, Q3_OUT, Q4_OUT
IBM 468x:	RS232_OUT1, OCIA_CLK_IN
WAND EMULATION:	B1_IN, Q4_OUT, Q5_OUT

31 RS-232 I/O Specification

This specification applies whenever the I/O signals are configured to be in RS-232 mode. Any detail not specified herein shall be defaulted to EIA/TIA-232E specification. The speed of serial transmission shall be no more than 120kilo-Bits-Per-Second. There are two transmit signals, TXD and RTS, and two receive signals, RXD and CTS. The output disable shall be provided so that these output pins can be shared among other functions.



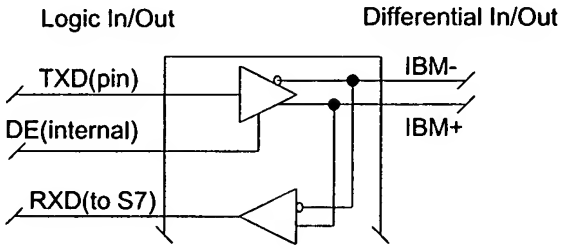
Electrical Specifications

Parameter	Typical	Unit	Condition
RS-232 output voltage swing	+/-3.5 min	V	Vcc = 5V, Rload = 3K Ohm
RS-232 output resistance	245 min	Ohm	~~Vcc = 0V, Vout = +/-2V~~
Slew Rate	4-30	V/us	Rload = 3K Cload = 1000PF, +3V to -3V
(note 1)Input Logic Threshold Low	0.8 max	V	
(note 1)Input Logic Threshold High	2.4 min	V	
(note 1)Logic Output High	3.7 min	V	VCC = 5V
(note 1)Logic Output Low	0.1 max	V	I = 10uA
RS-232 Input voltage range	+/-5	V	
RS-232 Input Threshold high	2.6 max	V	
RS-232 Input Threshold low	0.8 min	V	
RS-232 Input Hysteresis	0.2	V	
RS-232 Input Resistance	3K-7K	Ohm	
Baud Rate	120K	BPS	Rload = 3K Cload = 1000PF
Output Short Circuit Current	+/-25	mA	
Output Disable leakage Current	+/-10	uA	Rload = 54 Ohm, VCC=5.0V
Note: 1. Specifications are for simulation only.			

32 RS-485 I/O Specification

This specification applies whenever the I/O is configured to be in RS-485 mode. Any detail not specified herein shall be defaulted to the EIA/TIA-485E specification. This function shall provide a pair of differential signals for both transmitter and receiver as depicted in the next diagram. The output-enable control signal, DE, is an internally derived interface control function.

32.1 Pin Name Definitions



RXD: Receiver Output

DE: Data Drive Enable from logic decoder

TXD: Data In

IBM+/-: Differential Input/Output, which are denoted as A and B in the next two tables

Truth Table (Output)

TXD	DE	A	B
X	0	Hi-Z	Hi-Z
0	1	0	1
1	1	1	0
X: don't care Hi-Z : high-impedance			

Truth Table (Input)

A,B	RXD
A>B+0.2	1
B>A+0.2	0
input open	1

Electrical Specifications

Parameter	Typical	Unit	Condition
Differential Drive Output	2 min	V	Rload = 100 Ohm, VCC=5.0V
	1.5 min	V	Rload = 54 Ohm, VCC=5.0V

Parameter	Typical	Unit	Condition
Output Common-Mode Voltage	3 max	V	Rload = 54 Ohm, VCC=5.0V
Output Disable leakage Current	+/-10	uA	Rload = 54 Ohm, VCC=5.0V
Receiver Input Threshold	+/-0.2	V	
Recv Input Threshold Hysteresis	+/-50	mV	
(note 1)Logic Input Threshold Low	0.8 max	V	
(note 1)Logic Input Threshold High	2.4 min	V	
Receiver Logic Output High	3.7 min	V	VCC = 5V
Receiver Logic Output Low	0.1 max	V	I = 10uA
Receiver Input Resistance	500 min	Ohm	
Receiver Input CM Voltage	0-3	V	
Single ended output rise/fall time	15	ns	Rload = 54 Ohm, VCC=5.0V, Cload=100PF
Data Rate	200K	BPS	Rload = 500 Ohm, Cload = 5100 PF to Ground on both outputs, VCC=5.0V

33 The Differential Receivers

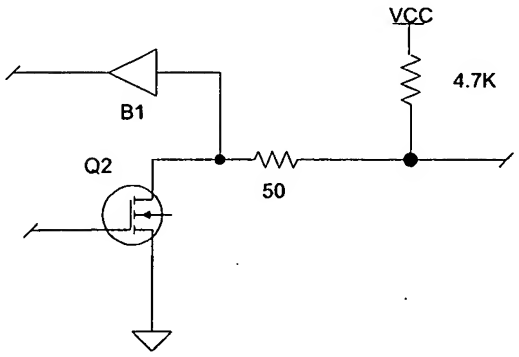
The receivers for OCIA input signals are using either the voltage comparators or input buffers that thresholds at 2.5V with adequate hysteresis. The RS-485 receiver is shared among the RS-485 and the OCIA signals.

Electrical Specifications

Parameter	Typical	Unit	Condition
OCIA input voltage	0 - 5	V	
OCIA output low	0.6max	V	I = 5mA
OCIA output high	4.5 – 5.2	V	VCC = 5V
OCIA data rate	300Kmax	Hz	
Recv. input Threshold Hysteresis	+/-50	mV	
(note 1)Propagation delay for both high-to-low and low-to-high	300max	ns	Input differential > 100mV
Note 1: parameters are specified for design simulation only. These parameters are not testable.			

34 The Discrete Drivers and Receivers

The discrete drivers and receivers are provided for implementation of Synapse, Wand Emulation, Keyboard Wedges and OCIA interfaces. The circuit uses open-drain FETs to drive data in either direction. A current limiting arrangement should be provided if the enclosed driver cannot tolerate a direct short to 5V DC.



Electrical Specifications

Parameter	Typical	Unit	Condition
I/O PAD Voltage Range	+/-5V	V	Only for Q1 and Q2 and B1 and B2
B1 Logic Input Threshold Low	0.8 max	V	
B1 Logic Input Threshold High	2.4 min	V	
(note 1)Logic Output High	3.7 min	V	VCC = 5V
(note 1)Logic Output Low	0.1 max	V	I = 10uA
Driver Sink Current	5 min	mA	Vout = 0.6V
Driver Leakage Current	10 max	uA	Vout = 5V
Output short circuit current	220	mA	Vout = 5V
(note 1)Propagation delay on B1	40	ns	Cload = 50pF
(note 1)Turn-on Time of Q2	40	ns	
(note 1)Turn-off Time of Q2	40	ns	
Note 1: parameters are specified for design simulation only. These parameters are not testable.			

35 The Analog Switches

The purpose of analog switches is to multiplex different interface signals in order to share the limited number of I/O pins. The implementation of any of the switches may not degrade or distort their associated signals (e.g. S6 or S14 may not clamp its signal to GND since the excursion of the signal is ±5V).

Electrical Specifications

Parameter	Typical	Unit	Condition
Logic Input Threshold Low	0.8 max	V	
Logic Input Threshold High	2.4 min	V	
Logic Output High	3.7 min	V	VCC = 5V
Logic Output Low	0.1 max	V	I = 10uA
Ron	35-160	Ohm	Vout = +5V or –5V

(note 1)Feed through Capacitance	0.5max	pF	
Switch Turn-on Time	30-200	ns	Rload = 1K, Cload = 50pF
Switch Turn-off Time	30-200	ns	Rload = 1K, Cload = 50pF
Note 1: parameters are specified for design simulation only. These parameters are not testable.			

The switches S10-S13 are to demonstrate the output disconnection abilities of both RS-232 and RS-485 output. It does not dictate what the actual implementation will be. The actual design can probably be done with an output disable feature in the output drivers.

36 Status indicator LED driver

The micro controlled status indicator LED driver shall be able to sink at least 10mA of current to the GND reference continuously.

37 Power down and Wakeup Detector

There are three power-down controls governed by the 8051 process. They are the control of the PLL oscillator, the –5V charge pump and the scanner power enable control. According to the USB 1.1 specification, a USB function allows a function device to draw less than 500uA of supply current during USB suspend, where as in the reset of interface modes, supply current of less than 1mA is generally desired. Therefore, in USB mode, the 8051 ~~has to~~must turn off both the PLL oscillator and the charge pump upon USB host suspension. Contrary, the charge pump will required to be on during RS-232 I/O mode. In order to meet this 1mA power requirement, both RS-232 output drivers need to be disabled during power down mode. That is done by the interface control decode to activate the RS_232_TXEN* signal to disable the RS-232 transmitters while the PLL is turned off. A power control override is provided to the external micro to disable the 8051 from controlling its power state.

The following on/off controls shall be provided for the power saving purposes:

- The –5V charge pump control (please refer to the interface control section for detail).
- The 1.84615MHz clock to the UART
- The 24MHz clock to the Micro
- The 48MHz clock to the USB SIE
- The power to the external (scanner) circuitry.

In order for the 8051 to control the power to the external micro and its own clock, two register each for both 8051 and external micro shall be provided. As is indicated, the 8051 can only read from the override register and the external micro can only read from the power state registers.

POWER CONTROL REGISTER (R/W) 8051 ADDR: 9420h

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R PWR	MIA PLL						

1: ON

0: OFF

Reset Default State is SCANNER PWR OFF and MIA PLL ON.

POWER OVERRIDE REGISTER (R) 8051 ADDR: 9421h

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R OVRIDE							

1: ON

0: OFF: Reset default

POWER STATE REGISTER (R) MIA ADDR: 0FH

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R PWR	MIA PLL						

1: ON

0: OFF

Reset Default State is SCANNER PWR OFF and MIA PLL ON.

POWER OVERRIDE REGISTER (R/W) MIA ADDR: 0EH

D7	D6	D5	D4	D3	D2	D1	D0
SCN'R OVRIDE							

1: ON: override the power control

0: OFF: leave the power control via the 8051, which is the Reset default state

The detection of wakeup event will re-start the PLL oscillator from its off state and subsequently resume the 8051 processor. Events that can be used to generate the wakeup signal are the following:

- USB resume signal detected from sensing the falling edge on DIP input out of the transceiver.
- RS-232/485 Start bit detected (high to low transition out of the RS-232 transceiver)
- RS-232 handshake signal (CTS) switching from high to low out of the transceiver.
- Synapse Remote request (host pull the SYN_CLK signal)
- The external wakeup events, such as scan stand switch or trigger switch etc.
- OCIA Data detected from sensing the low to high transition on the OCIA_CLKOUT signal.

Provision shall be made to allow or disallow individual event from generating a wake up signal. Once the appropriate wakeup signal is detected, it will subsequently generate a wakeup output to be used by the external circuit such as the scanner micro.

WAKEUP MASK CONTROL REGISTER (R/W) ADDR: 940Eh

D7	D6	D5	D4	D3	D2	D1	D0
USB DIP	IBM 468X	OCIA CLKO	EXT WAKUP	SYN		CTS	UART RXD

1: ENABLE

0: DISABLE : all 0 after external reset

WAKEUP STATUS REGISTER (R) ADDR: 940Fh

D7	D6	D5	D4	D3	D2	D1	D0
USB DIP	IBM 468X	OCIA CLKO	EXT WAKUP	SYN		CTS	UART RXD

1: ENABLE

0: DISABLE : all 0 after external reset

38 Download Detector

The download detector is an invert buffer that flows directly out to the external processor. Once the download enable is detected, the chip will retain the following states:

- 8051 will be put in its reset state.
- Interface selection will be overrides to RS-232.
- The Charge Pump will remain on regardless.
- The Scanner power control will be enabled at all time.
- The RS-232 TXD and RXD signals are by-passed to the external processor.

39 3.3V Regulator

The 3.3V Regulator output is used to power the USB core and USB transceiver. A 4.7uF low-ESR tantalum capacitor shall be used to stabilize the voltage regulator. **This 3.3V regulator is designed for internal use only. No external use of this 3.3V regulator output is recommended.**

40 Development Tools

At least the following development tools shall be made available prior to the beginning of the ASIC development. Development board (evaluation prototype) can be a plus to shorten the development time but it is not mandated.

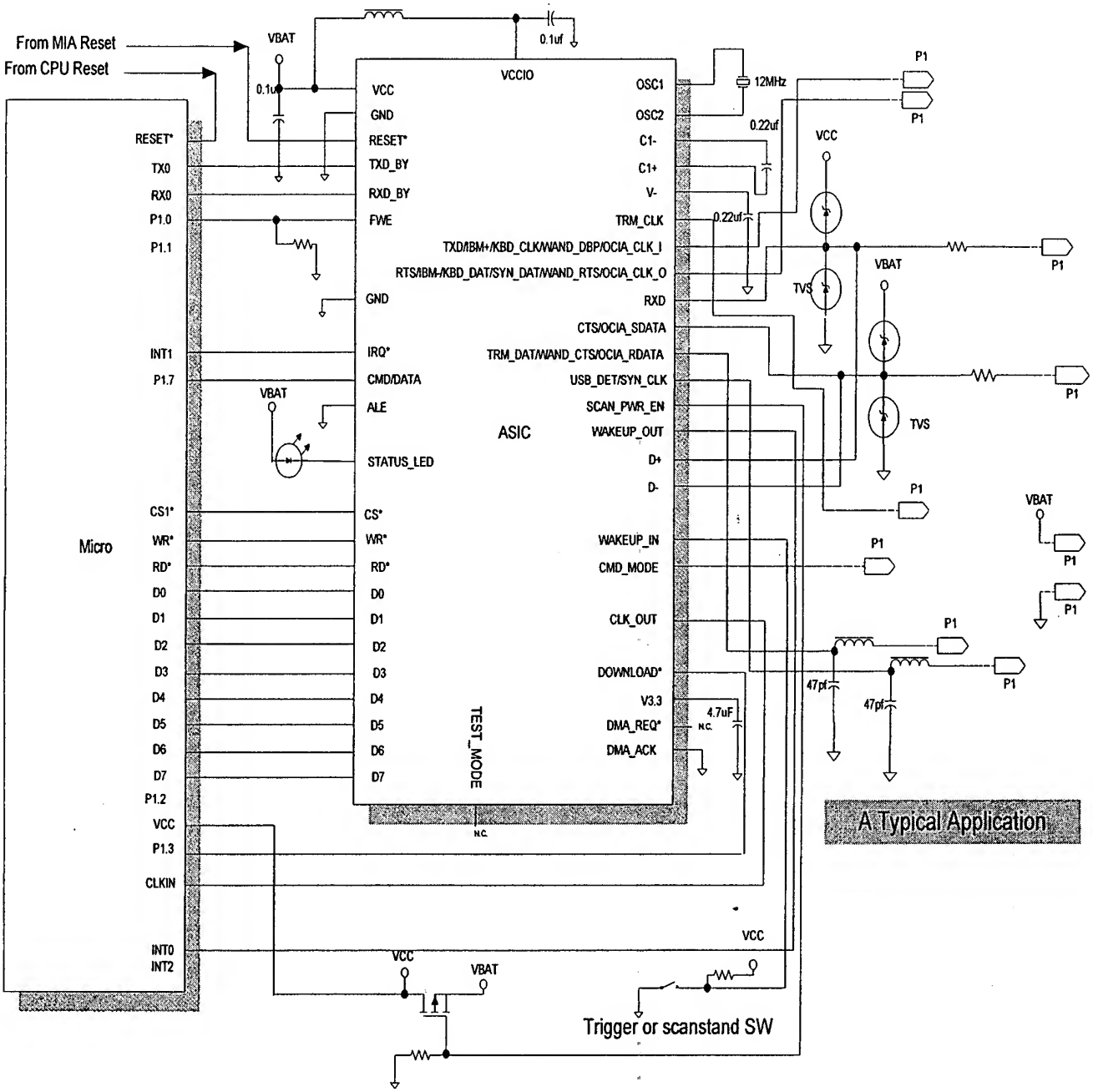
- The development suite (C compiler, Assembler, Linker are musts, but the simulator is optional).
- The In-Circuit Emulator for the micro. A special bond-out chip with additional I/O pins for ICE is a must for software development.

41 Fault Coverage

The fault coverage for the production version of the ASIC has to be better than 95%.

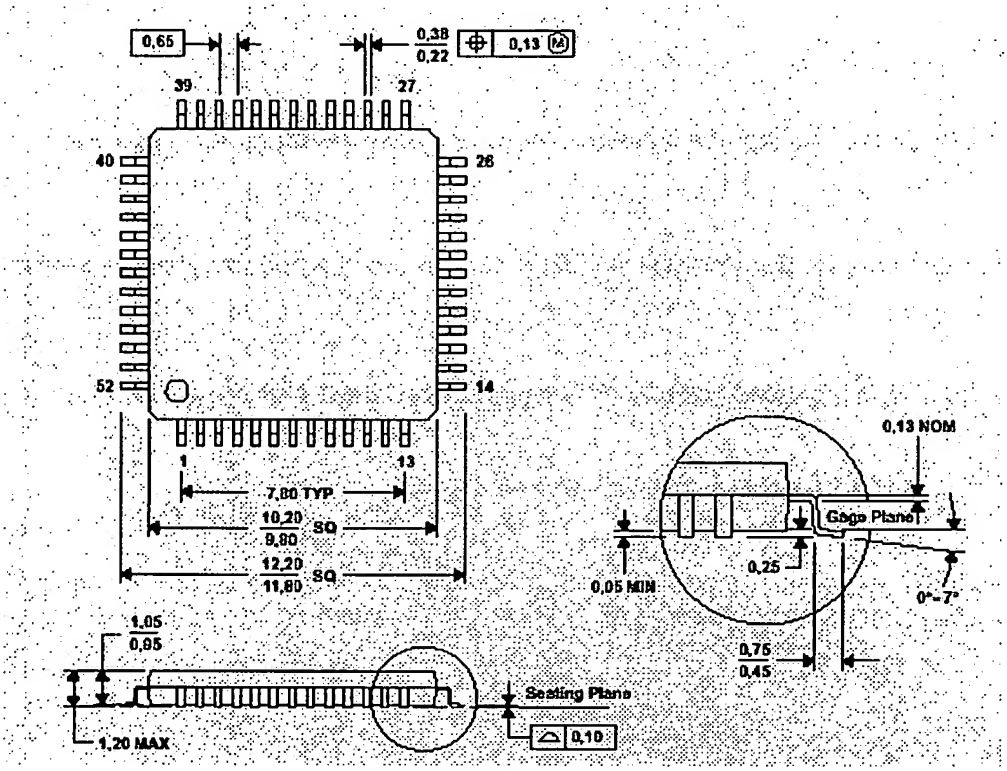
42 Typical Application and Interconnection

A typical application of this ASIC is illustrated in the following diagram.


From MIA Reset
From CPU Reset
VBAT
0.1uf
VCCIO
VCC
GND
RESET*
TXD_BY
RXD_BY
FWE
IRQ*
CMD/DATA
ALE
STATUS_LED
CS*
WR*
RD*
D0
D1
D2
D3
D4
D5
D6
D7
TEST_MODE
N.C.
ASIC
OSC1
OSC2
C1-
C1+
V-
TRM_CLK
TXD/IBM+/KBD_CLK/WAND_DBP/OCIA_CLK_I
RTS/IBM-/KBD_DAT/SYN_DAT/WAND_RTS/OCIA_CLK_O
RXD
CTS/OCIA_SDATA
TRM_DAT/WAND_CTS/OCIA_RDATA
USB_DET/SYN_CLK
SCAN_PWR_EN
WAKEUP_OUT
D+
D-
WAKEUP_IN
CMD_MODE
CLK_OUT
DOWNLOAD*
V3.3
DMA_REQ*
DMA_ACK
12MHz
0.22uf
4.7uF
N.C.
47pf
TVS
P1
Micro
RESET*
TX0
RX0
P1.0
P1.1
INT1
P1.7
CS1*
WR*
RD*
D0
D1
D2
D3
D4
D5
D6
D7
P1.2
VCC
P1.3
CLKIN
INT0
INT2
Trigger or scanstand SW
A Typical Application

4243 Package

The standard chip should be packaged in the smallest package possible, considering both thermal dissipation and cost impact. The preferred packages are TQFP52.



For the special bound-out chip, a 121-pin PGA ceramic package will be used.

4344 Marking

TBD

4445 Temperature Range

Operating: -40 to 85°C

Storage: -65 to 120°C

4546 Compliance

Considering the regulatory requirements for those applications that this device will be integrate in, the device will be subjected to the following tests. Hence, the design of this device shall pass these test requirements.

4647 ESD

±8KV on the following dedicated I/O signals.

1. TXD/IBM+/KBD_CLK/WAND_DBP/OCIA_CLK_I
2. RTS/IBM-/KBD_DAT/SYN_DAT/WAND_RTS/OCIA_CLK_O
3. RXD
4. CTS/OCIA_SDATA

Measure the radiated field from the unit over the frequency range 30MHz to 1GHz, as per C.I.S.P.R. Class B test conditions.

Radiated and Conducted EMI Susceptibility: Expose the unit to 10 V/m over the frequency ranges 10kHz to 1GHz.

Electro-Fast Transients (EFT Burst): Subject cable to ±1kV amplitude and 5kHz high current interference.

Transient Susceptibility: Inject 150ns and 50us transient on the DC lines.

EXHIBIT K

Program Milestones	Plan	Comments
Design Kickoff	12/2	
Preliminary Design Review	12/13	
Symbol Net list to UTMC	2/23	UTMC claims there may be 3 week slip due to a personnel issue. Working to minimize overall impact. They are finalizing I/O design.
S/W Design Doc/Rev	3/23	S/W Dates are preliminary and looking to improve them
S/W Coding/ and unit test	7/20	Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	4/30	
ASIC Proto Fab (start)	5/8	Will need to order qty to cover Alpha/pilot builds
Protos Received	7/15	May be able to improve date with $'s, ICE version earlier
H/W S/W Integration & Testing	8/2	
S/W Validation	8/30	
Proto Acceptance	8/15	
Major Mfg. Milestones		
Risk Production availablity	8/15	
Qual Completion	TBD	Final Product dependent
Rev A Release	8/31	Component Level & S/W
Initial production Start	8/31	UTMC will build additional wafers at proto time to reduce lead time days

EXHIBIT L

The cross-reference signal names between net-list and MIA specification

The digital signal names are list as following:

Pad name	Net-list Signal Name	I/O
A0	CMD/DATA	In
RESET*	RESET_N	In
RSV1	RSV1	InOut
POF_INT	SOF	Out
WAKEUP_IN	SCANSTAND	In
SCAN_PWR_EN	SUSPEND	Out
WAKEUP_OUT	WAKEUP	Out
FWE	FWE	In
CS*	CS_N	In
WR*	WR_N	In
RD*	RD_N	In
D0-7	D9-7	InOut
RESET*	RESET_N	In
TEST	TEST	In
ALE	ALE	In
TXD_BY	TXD_BY	In
RXD_BY	RXD_BY	Out
DMA_REQ*	DMA_REQ	Out
DMA_ACK	DMA_ACK	In
EOT*	EOT_N	Out
IRQ*	IRQ_N	Out
CLK_OUT	CLK_OUT	Out
DOWNLOAD*	DOWNLOAD_N	Out

So far, there is only one reserved pin remaining (RSV1) in the design, which is tie internally to 8051's TXD1 (P1.3), the intent is to make it either as UART output for debug or a bi-directional port pin whenever needed. Originally, there were three reserved pins. One of them got converted to VCCIO and the other one turned into the POF_INT.

The signals that associated with the internal analog blocks is listed as the following:

Net-list Signal name	Description	Active State
FCLK	48Mhz clock	
PLL_ON_OFF	the control to turn PLL on/off	High is on, low is off
RES_IN	the pull up resistor control	High is in, low is out
N_TG_EN	the USB TG enable control	Low is on, high is off
CP_ON	the –5V charge pump control	High is on, low is off
USB_CONN	the USB connect control	High is on, low is off
USB_SUSPEND	the USB suspend signal	High is suspend
N_RS_485_OE	RS485_OE	High is enable
N_RS_232_TXEN	RS_232_TXEN*	Low is enable

N_RS_232_TXEN	RS_232_TXEN*	Low is enable
OCIA_EN	OCIA_EN (spec)	High is enable
KBD_WAND_EN	KBD_WAND_EN (spec)	High is enable
SYN_EN	SYN_EN (spec)	High is enable
KBD_CLOSE	KBD_CLOSE (spec)	High is enable
N_DOWNLOAD	DOWNLOAD*(spec analog)	
RS232_OUT1	RS232_OUT1 (spec)	Output
RS232_OUT2	RS232_OUT2 (spec)	Output
RS232_IN1	RS232_IN1 (spec)	Input
RS232_IN2	RS232_IN2 (spec)	Input
Q1_OUT1	Q1_OUT1 (spec)	Output
Q2_OUT1	Q2_OUT1 (spec)	Output
Q3_OUT1	Q3_OUT1 (spec)	Output
Q4_OUT1	Q4_OUT1 (spec)	Output
Q5_OUT1	Q5_OUT1 (spec)	Output
B1_IN	B1_IN (spec)	Input
B2_IN	B2_IN (spec)	Input
B3_IN	B3_IN (spec)	Input
OCIA_CLKOUT	OCIA_CLK_OUT (spec)	Input
OCIA_CLKIN	OCIA_CLK_IN (spec)	Input
OCIA_SDATA	OCIA_SD_IN (spec)	Input

The MULTITOP is the top level of the MIA digital design. It consists of MULTIWRAP52, ANALOG_IO and IO_BUFFERS52 components. The ANALOG_IO and IO_BUFFERS52 are just components that instantiated the I/O cells from Hyundai libraries. Most of the signals of the MULTIWRAP52 are either in or out except those signals that make up the D0-7 and RSV1 described earlier. The D_IN0-7 and D_OUT0-7 are input and output signals of D0-7controlled via the D_OUT_EN signal. The RSV1_EN is the output enable control for RSV1_OUT and its input equivalent is P13_IN.

EXHIBIT M

Multi-Interface ASIC (MIA) Overview

Presented to PSC
March 20, 2001

Symbol Technologies
Confidential

MIA Overview

- MIA Developers
- Why MIA?
- Goals of Implementation
- MIA Technical Challenges
- System Overview, Operation and Implications
- Schedule
- MIA is not ...
- Operations Issues
- Program Issues
- Summary

MIA Developers

- Tony Chang
- John Fioriglio
- Rizwan Alladin
- Brad Morris
- Rob Lieb
- Others to be added shortly....

Why MIA?

- Channel Partners, Operations, and Engineering desire to minimize configurations.
- Marketing desire to support Multi-Interface capability at a low cost point.
- Competitors offered channel friendly multi-interface solutions

Why MIA?

- Current Multi-Interface Solutions
  - Example using the LS 400Xi
    - LS4004i --- RS232, Synapse
    - LS4005i --- IBM4683, Synapse
    - LS4006i --- Keyboard Wedge, Synapse

      Total of three configurations
  - LS4005i, LS4006i, M2005, M2007 and LS6005 all use the Synapse uP to integrate respective interface
    - Additional Cost ~$3.00
  - Synapse Model – Additional cost > $20

MIA Goals

- Cost Effective Solution – Target Cost $3.25
- Leverage Previous Interface Work
  - The "Synapse Benefit"
- Support Most Popular Interfaces
  - RS 232
  - P/S 2 Kybd
  - USB
  - IBM 46XX
  - Wand
  - Synapse

MIA Goals (cont.)

- ⌘Provide flexibility supporting multiple interface variants (e.g.int'l kybds)
- ⌘Work with multiple decoder architectures
- ⌘Minimize development costs both capital costs and recurring Engineering development efforts
- ⌘Provide clean partition between interface and decoder S/W

MIA Technical Challenges

- Development of Mixed Mode ASIC
- Embedded Core w/Flash
- Development Environment
  - How does an ICE work with this device
- Use existing Universal Cables
- Ensure no damage for "incorrect installations"

MIA System Overview

- Embedded DW51 Core
  - 8031 uP derivative used in IMP
  - Similar architecture to Synapse uP
- 32K embedded Flash
- 2K RAM
- USB Interface controller
- Analog/Digital Interface Circuitry

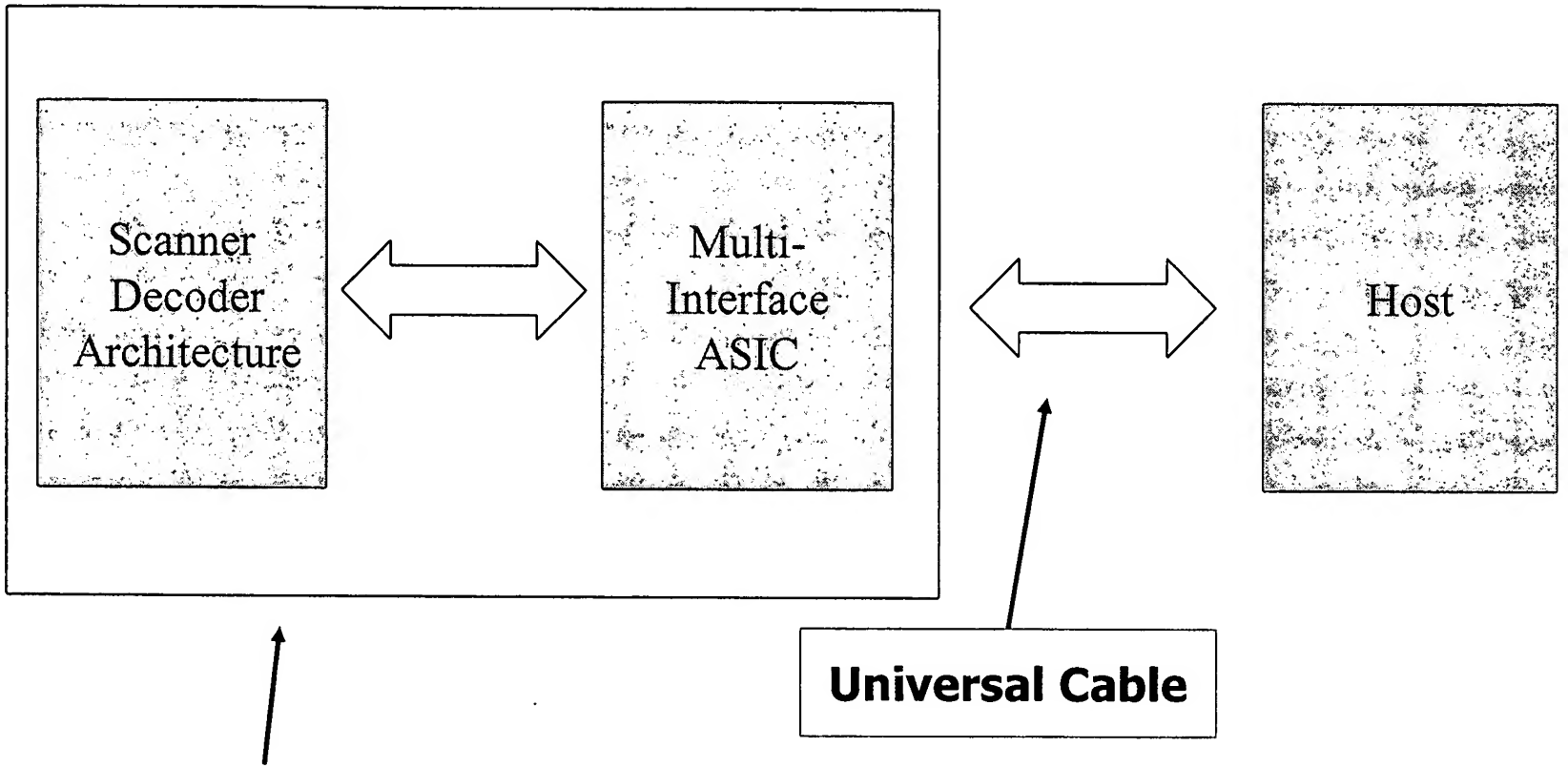
MIA Features

- Supported Interfaces
  - RS232 (EIA levels, +/- 5 volts, 115 Kbaud)
  - USB (Bulk, Interrupt and Isochronous)
    - HID Keyboard Emulation
    - IBM Yellowstone
    - Symbol's Proprietary Implementation (Keystone)
  - PS/2 Keyboard Emulation
  - Wand Emulation
  - RS485
  - Synapse
  - Flash Download Capability

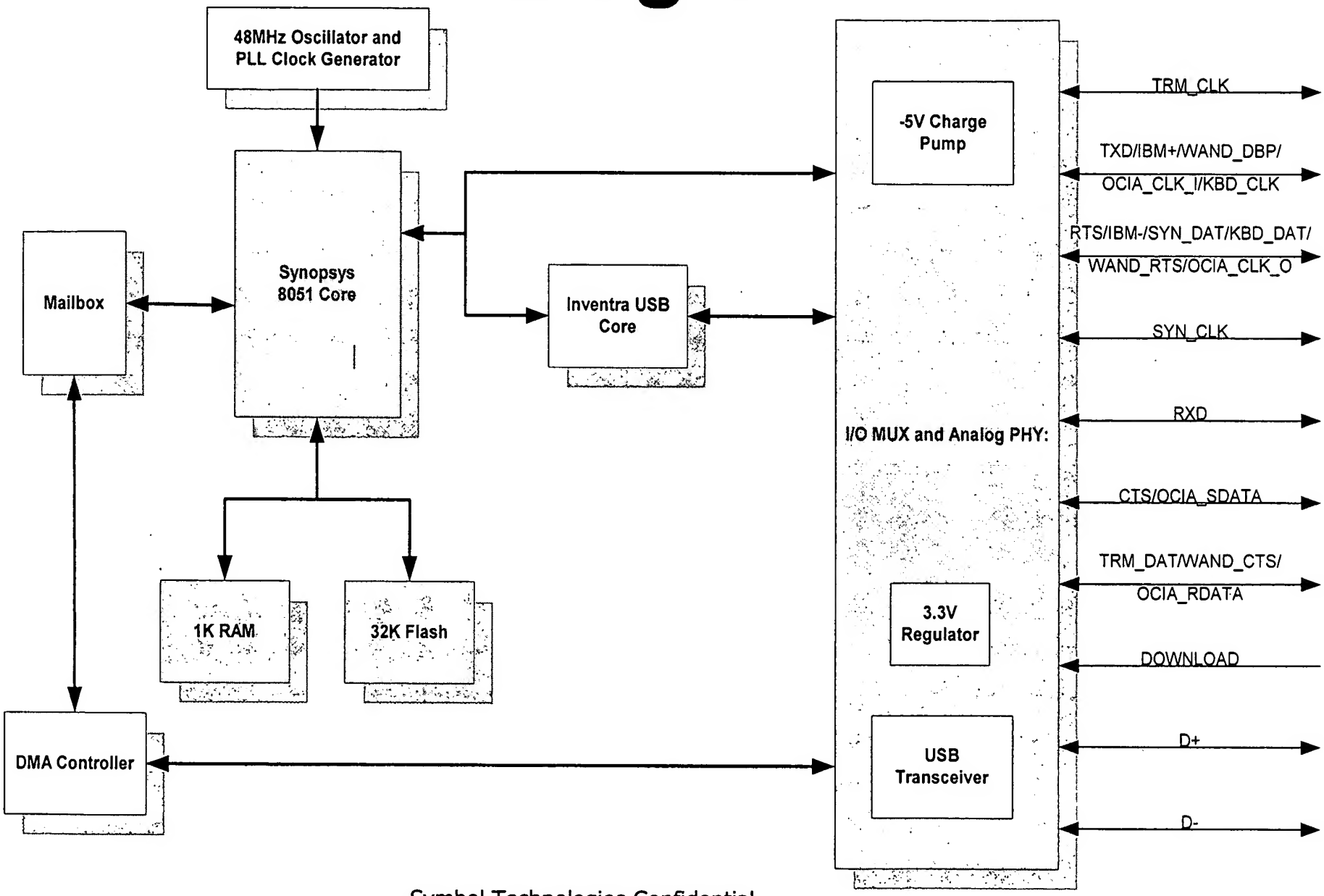
MIA Features

- 5 Volt Vcc
- Packaged in a 52 pin TPQFP
- Mixed Mode (RS232 charge pump, USB engine, 3.3V Regulator, Interface Multiplexing)
- ASIC expected to be used in multiple scanner programs

Scanner with MIA Overview

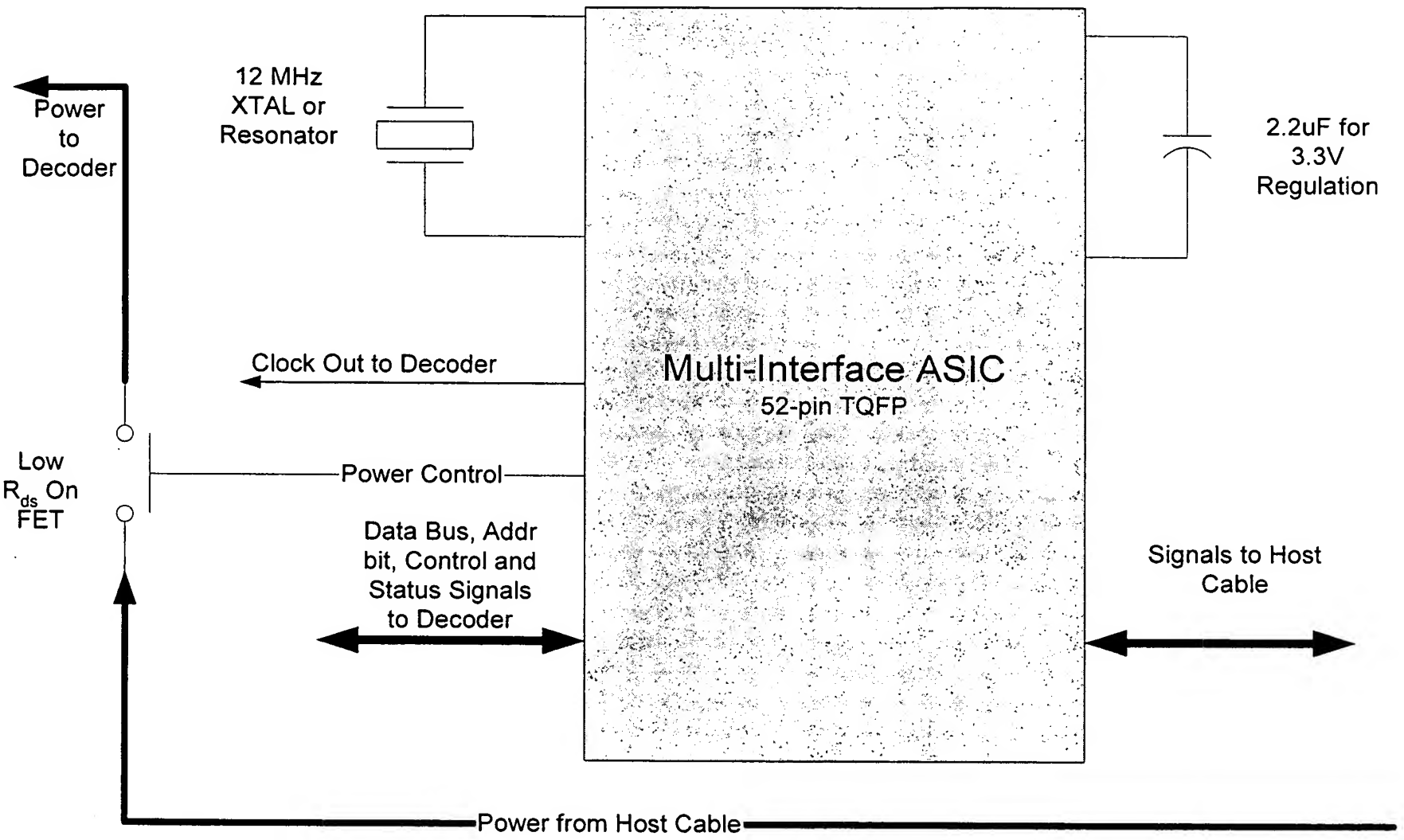


MIA Block Diagram



Symbol Technologies Confidential

What external circuitry does MIA need?



Integration Implications

- Software
  - Significant effort to port interfaces to MIA environment.
  - Scan/decode and interface software will have to co-exist on same core
  - Current Flash Download utility will have to be enhanced
  - Significant effort to re-validate Interface code.

Integration Implications

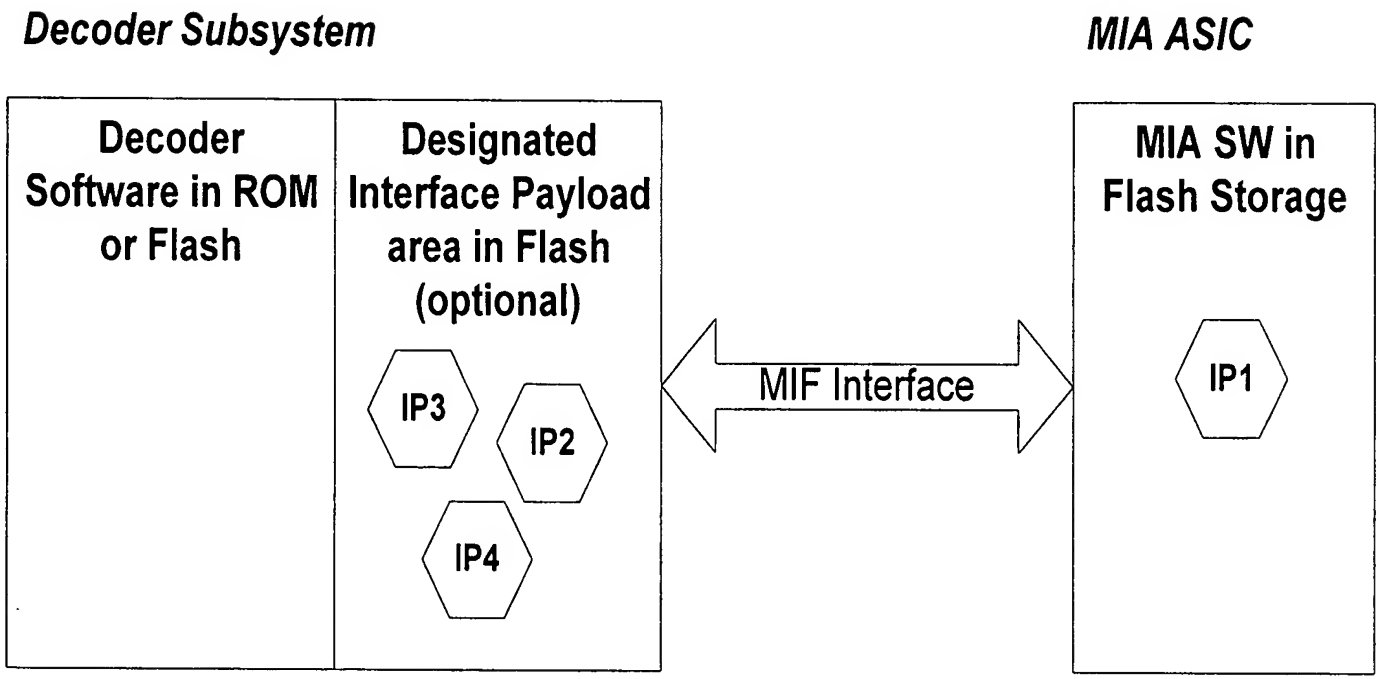
- Hardware
  - Future platforms will need necessary code space to support all the interface combinations.
  - More port pins needed to interface to proposed ASIC. (Worse Case = 8)
  - USB implementation may still require external logic to meet stringent current draw requirements.

MIA Initial Operation –

"Taking a book from the Library"

- Scanner is downloaded in factory (Decoder and I/F S/W in same image)
- Interface is selected/programmed in scanner
- Correct I/F image is downloaded to MIA flash

MIA Interface Payload



Flash Downloading w/ MIA

- Flash download is transparent to MIA
- Flash download cable attached to product
- MIA Processor held in reset
- Hex Image is loaded to decoder Flash

Interface Switching – 3 Conditions

- I/F code not available in Scanner or MIA
  - User is given error beeps
  - Needs to install intended I/F code from ...
- I/F code available in MIA*
  - Decoder sends "Reset Request"
  - MIA activity suspended
  - Decoder updates MIA settings

Interface Switching (cont'd.)

- I/F code available in Scanner* (I/F Payload Area)
  - Decoder sends "Reset Request"
  - MIA activity suspended
  - Decoder updates MIA Flash image
  - Decoder updates MIA settings

Interface Switching

- Changing I/F will not damage electronics, but may cause gibberish on signal lines to host
- Suggested behavior for changing host types (e.g. RS-232 to USB)
  - System install temporary null host
  - On power up (after cable change), new host is installed
- Comments????? (especially you Marketing folks!)

Scanner w/MIA : Normal Operation

- Scanner decodes barcode
- ADF (if enabled) is performed
- Decoder transfers data to MIA via mailbox (MIF)
- MIA formats data and sends to the host

Actually, this is a lot like Synapse and the SDCI protocol!

MIA Development Environment

- Currently developing FPGA development system
- Creating Bond out version of the device
  - All uP pins are external
  - 1 in 6 die/wafer
  - Packaged in 120 PGA package

MIA / Scanner Utilities

- Late customization capabilities
- Adding new / alternate Interface code (Interface Payload Configuration Utility)
- Scanner Configuration Utility for default parameter selection and storage
- Flash Download utility

Schedule Milestones

Program Milestones	Plan	Comments
Design Kickoff	12/2	
Preliminary Design Review	12/13	
Symbol Net list to UTMC	3/9	
S/W Design Doc/Rev	3/23	S/W Dates are preliminary and looking to improve them
S/W Coding/ and unit test	7/20	Keybd. Wdg., Rs-232, Synapse, IBM, Wand, SPCI, USB
ASIC Critical Design Review	4/30	
ASIC Proto Fab (start)	5/8	Will need to order qty to cover Alpha/pilot builds
Protos Received	7/15	May be able to improve date with $'s, ICE version earlier
H/W S/W Integration & Testing	8/2	
S/W Validation	8/30	
Proto Acceptance	8/15	
Major Mfg. Milestones		
Risk Production availablity	8/15	Protos available prior
Qual Completion	TBD	Final Product dependent
Rev A Release	8/31	Component Level & S/W

MIA Status

- Preliminary netlist transferred to vendor 3/9
- FPGA Development board in debug
- Preliminary High Level System S/W design completed 3/16
- On-site design review scheduled 4/12, CDR 4/30

What Not to Expect

- Interfaces not supported: Legacy Systems, OCIA (actually H/W is in ASIC)
- Cost burdens less expensive interfaces.
  - Example:
    - Keyboard Wedge-only solution = ~$0.50
    - Keyboard Wedge solution via ASIC > $3.00
  - The single dedicated interface is always the lowest cost solution

What Not to Expect (cont'd.)

- May not be viable solution for all scanner products
  - Costly for low-end consumer products
  - Will not support USB 2.0 high speed data transfer rates (up to 480 Mbits/second)

Operations Issues

- Unique ID for USB programmed at Manufacture (similar to RL 474/5)
- Capability to program/select interface at time of packaging
- Default MIA payload – what will it be?
- Appropriate testing – not all possible interfaces, but an intelligent subset

Program Issues

- Schedule is very tight for all PSC variants – first silicon success required
- Power Scan variant poses potential issues with use of existing PSC cables
- All products should have PCB waiting to drop in MIA prototypes
- Need forecast for Alpha qty's and Q4 usage !!!

What will Symbol provide PSC to enable them to create *Interface Payloads*

- System Documentation for H/W and S/W (After internal release April)
  - ☒ Symbol's SMI (Scanner MIA Interface) Interface (Rev. 0.9)
  - ☒ Symbol's MIF (Mailbox Interface) Interface (Rev. 0.9)
  - ☒ Multi-Interface ASIC Specification (Rev. 5)
- Development PCB
  - ☒ FPGA Based – April 30th
  - ☒ Bond out chip based – August time-frame

What will Symbol provide PSC to enable them to create *Interface Payloads and customize scanners (cont'd)*

- PC Based utilities
  - Scanner Configuration Utility
  - Interface Payload Configuration Utility
  - Flash Download Utility

What PSC will need to provide to create *Interface Payloads*

- Provide DW 51 compatible ICE and appropriate adapters for use with development PCBs
- Need forecasts for pilot and first quarter volumes
- Common USB Strategy for Comm/Serial ports*

* Not really a need, but there is an opportunity here to set a standard

MIA Summary

- A significant effort for both H/W and S/W
- A flexible, cost effective solution for multi-interface applications
- A re-usable design to be deployed in future scanners as easily as Synapse

MIA Overview – The End!

⌘Questions ?

EXHIBIT N

PAD	Direction	Cell	Pins	Pin on cell	Pin on MULTICORE
WAKEUP_IN	Input	PSIT0	Y	SCAN_STAND	SCAN_STAND
WDT_INH	Input	PSIT0	Y	EXT_WDT_INH	EMU_WDT_INH
EMULATE	Input	PSIT0	Y	EMU_EN	EMULATE_EN
TEST	Input	PSIT0D	Y	TEST_EN	TEST
FWE	Input	PSIT0D	Y	FLASH_WR_EN	FWE_IN
RESET_N	Input	PSIT0U	Y	RESET	RESET
CMD_DATA	Input	PSIT0	Y Pad	A0_IN A0	A0
ALE	Input	PSIT0	Y	ALE_IN	ALE
CS_N	Input	PSIT0U	Y	CS	CS
WR_N	Input	PSIR0	Y	WR	WR
RD_N	Input	PSIT0	Y	RD	RD
TXD_BY	Input	PSIT0	Y	TXD_BYPASS	TXD_BY
P1_3	Input	PSIT0	Y	EMU_P13_IN	EMU_P13_IN
DMA_ACK	Bidir	PSB3R0	A EN Y	PORT3_OUT(3) DMA_ACK_EN DMA_ACK_SDCI_CLK_IN	PORT3_OUT(3) DMA_ACK_EN DMA_ACK_SDCI_CLK_IN
DMA_REQ	Bidir	PSB3R0	A EN Y	DMA_REQUEST DMA_REQ_EN P15_IN	DMA_REQ DMA_REQ_EN P15_IN

CPSEN	Bidir	PSB3R0	A	CPU_PSEN	CPU_PSEN
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_PSEN	EMU_PSEN
CALE	Bidir	PSB3R0	A	MEM_ALE	MEM_ALE
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ALE	EMU_ALE
CRD_N	Bidir	PSB3R0	A	CPU_RD	CPU_RD
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_MEM_RD	EMU_MEMR
CWR_N	Bidir	PSB3R0	A	CPU_WR	CPU_WR
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_MEM_WR	EMU_MEMW
AD0	Bidir	PSB3R0	A	AD_A(0)	AD_A(0)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(0)	EMU_AD_IN(0)
AD1	Bidir	PSB3R0	A	AD_A(1)	AD_A(1)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(1)	EMU_AD_IN(1)
AD2	Bidir	PSB3R0	A	AD_A(2)	AD_A(2)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(2)	EMU_AD_IN(2)
AD3	Bidir	PSB3R0	A	AD_A(3)	AD_A(3)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(3)	EMU_AD_IN(3)
AD4	Bidir	PSB3R0	A	AD_A(4)	AD_A(4)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(4)	EMU_AD_IN(4)

AD5	Bidir	PSB3R0	A	AD_A(5)	AD_A(5)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(5)	EMU_AD_IN(5)
AD6	Bidir	PSB3R0	A	AD_A(6)	AD_A(6)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(6)	EMU_AD_IN(6)
AD7	Bidir	PSB3R0	A	AD_A(7)	AD_A(7)
			EN	AD_EN	AD_EN
			Y	EXT_AD_IN(7)	EMU_AD_IN(7)
A8	Bidir	PSB3R0	A	CPU_ADDR(8)	CPU_ADDR(8)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(8)	EMU_ADDR_IN(8)
A9	Bidir	PSB3R0	A	CPU_ADDR(9)	CPU_ADDR(9)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(9)	EMU_ADDR_IN(9)
A10	Bidir	PSB3R0	A	CPU_ADDR(10)	CPU_ADDR(10)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(10)	EMU_ADDR_IN(10)
A11	Bidir	PSB3R0	A	CPU_ADDR(11)	CPU_ADDR(11)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(11)	EMU_ADDR_IN(11)
A12	Bidir	PSB3R0	A	CPU_ADDR(12)	CPU_ADDR(12)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(12)	EMU_ADDR_IN(12)
A13	Bidir	PSB3R0	A	CPU_ADDR(13)	CPU_ADDR(13)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(13)	EMU_ADDR_IN(13)
A14	Bidir	PSB3R0	A	CPU_ADDR(14)	CPU_ADDR(14)

			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(14)	EMU_ADDR_IN(14)
A15	Bidir	PSB3R0	A	CPU_ADDR(15)	CPU_ADDR(15)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EXT_ADDR_IN(15)	EMU_ADDR_IN(15)
P1_1	Bidir	PSB3R0	A	PORT1_OUT(1)	PORT1_OUT(1)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EMU_P11_IN	EMU_P11_IN
P1_6	Bidir	PSB3R0	A	PORT1_OUT(6)	PORT1_OUT(6)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EMU_P16_IN	EMU_P16_IN
P3_1	Bidir	PSB3R0	A	PORT3_OUT(1)	PORT3_OUT(1)
			EN	EMULATE_EN_N	EMULATE_EN_N
			Y	EMU_P31_IN	EMU_P31_IN
D0	Bidir	PSB3R0	A	D_OUT(0)	D_OUT(0)
			EN	D_OUT_EN	D_OUT_EN
			Y	D_IN(0)	D_IN(0)
D1	Bidir	PSB3R0	A	D_OUT(1)	D_OUT(1)
			EN	D_OUT_EN	D_OUT_EN
			Y	D_IN(1)	D_IN(1)
D2	Bidir	PSB3R0	A	D_OUT(2)	D_OUT(2)
			EN	D_OUT_EN	D_OUT_EN
			Y	D_IN(2)	D_IN(2)
D3	Bidir	PSB3R0	A	D_OUT(3)	D_OUT(3)
			EN	D_OUT_EN	D_OUT_EN
			Y	D_IN(3)	D_IN(3)
D4	Bidir	PSB3R0	A	D_OUT(4)	D_OUT(4)
			EN	D_OUT_EN	D_OUT_EN

			Y	D_IN(4)	D_IN(4)
D5	Bidir	PSB3R0	A	D_OUT(5)	D_OUT(5)
			EN	D_OUT_EN	D_OUT_EN
			Y	D_IN(5)	D_IN(5)
D6	Bidir	PSB3R0	A	D_OUT(6)	D_OUT(6)
			EN	D_OUT_EN	D_OUT_EN
			Y	D_IN(6)	D_IN(6)
D7	Bidir	PSB3R0	A	D_OUT(7)	D_OUT(7)
			EN	D_OUT_EN	D_OUT_EN
			Y	D_IN(7)	D_IN(7)
RSV1	Bidir	PSB3R0	A	PORT1_OUT(3)	PORT1_OUT(3)
			EN	RSV1_EN	RSV1_EN
			Y	P13_IN	P13_IN
RSV2	Bidir	PSB3R0	A	PORT1_OUT(2)	PORT1_OUT(2)
			EN	RSV2_EN	RSV2_EN
			Y	P12_IN	P12_IN
SCAN_PWR_EN_N	Output	PS02M	A	SUSPEND_TEMP	SUSPEND
WAKEUP_OUT	Output	PS02M	A	EXT_WAKEUP	EXT_WAKEUP
IRQ_N	Output	PS02M	A	INT	INT
EOT_N	Output	PS02M	A	EOT	EOT
CLK_OUT	Output	PS02M	A	DEC_CLKOUT	CLK_OUT
RXD_BY	Output	PS02M	A	RXD_BYPASS	RXD_BY
P1_0	Output	PS02M	A	BAUD_CLK	BAUD_CLK
P1_2	Output	PS02M	A	P12_OUT	P12_OUT

P1_4	Output	PS02M	A	P14_IN	P14_IN
P1_5	Output	PS02M	A	PORT1_OUT(5)	PORT1_OUT(5)
P1_7	Output	PS02M	A	P17_IN	P17_IN
P3_0	Output	PS02M	A	PORT3_IN(0)	PORT3_IN(0)
P3_2	Output	PS02M	A	PORT3_IN(2)	PORT3_IN(2)
P3_3	Output	PS02M	A	PORT3_IN(3)	PORT3_IN(3)
P3_4	Output	PS02M	A	PORT3_IN(4)	PORT3_IN(4)
P3_5	Output	PS02M	A	PORT3_IN(5)	PORT3_IN(5)
POF_INT	Output	PS02M	A	SOF_TOGGLE	SOF
DOWNLOAD_N	Output	PS02M	A	N_DOWNLOAD	
COSC	Output	PS02M	A	CPU_OSC	COSC

Analog Signals

PAD	Direction	Cell	Pins	Pin on cell	Pin on MULTICORE
DIP_TEMP	Input	PSIT0	Y	DIP	DIP
DIM_TEMP	Input	PSIT0	Y	DIM	DIM
B1_IN_TEMP	Input	PSIT0	Y	B1_IN	B1_IN
DIDIF_TEMP	Input	PSIT0	Y	DIDIF	DIDIF
OCIA_CLKOUT_TEMP	Input	PSIT0	Y	OCIA_CLKOUT	OCIA_CLKOUT

B2_IN_TEMP	Input	PSIT0	Y	B2_IN	B2_IN
B3_IN_TEMP	Input	PSIT0	Y	B3_IN	B3_IN
OCIA_CLKIN_TEMP	Input	PSIT0	Y	OCIA_CLKIN	OCIA_CLKIN
OCIA_SDATA_TEMP	Input	PSIT0	Y	OCIA_SDATA	OCIA_SDATA
N_DOWNLOAD_TEMP	Input	PSIT0	Y	N_DOWNLOAD	N_DOWNLOAD
RS232_IN2_TEMP	Input	PSIT0	Y	RS232_IN2	RS232_IN2
RS232_IN1_TEMP	Input	PSIT0	Y	RS232_IN1	RS232_IN1
FCLK	Input	PSIT0	Y	FCLK_TEMP	FCLK_IN
N_TG_EN_TEMP	Output	PS02M	A	N_TG_EN	USB_XMIT_OUT
RES_IN_TEMP	Output	PS02M	A	RES_IN	RESISTORS_IN
DOP_TEMP	Output	PS02M	A	DOP	DOP
DOM_TEMP	Output	PS02M	A	DOM	DOM
NDOE_TEMP	Output	PS02M	A	NDOE	NDOE
Q5_OUT_TEMP	Output	PS02M	A	Q5_OUT	Q5_OUT
N_RS232_TEN_TEMP	Output	PS02M	A	N_RS232_TEN	N_RS232_TEN
RS232_OUT1_TEMP	Output	PS02M	A	RS232_OUT1	RS232_OUT1
RS232_OUT2_TEMP	Output	PS02M	A	RS232_OUT2	RS232_OUT2
CP_ON_TEMP	Output	PS02M	A	CP_ON	CP_ON

RS485_OE_TEMP	Output	PS02M	A	RS485_OE	RS485_OE
SYN_EN_TEMP	Output	PS02M	A	SYN_EN	SYN_EN
KBD_WAND_EN_TEMP	Output	PS02M	A	KBD_WAND_EN	KBD_WAND_EN
N_RS232_REN_TEMP	Output	PS02M	A	N_RS232_REN	N_RS232_REN
USB_CONN_TEMP	Output	PS02M	A	USB_CONN	USB_CONN
KBD_CLOSE_TEMP	Output	PS02M	A	KBD_CLOSE	KBD_CLOSE
Q1_OUT_TEMP	Output	PS02M	A	Q1_OUT	Q1_OUT
Q2_OUT_TEMP	Output	PS02M	A	Q2_OUT	Q2_OUT
Q3_OUT_TEMP	Output	PS02M	A	Q3_OUT	Q3_OUT
Q4_OUT_TEMP	Output	PS02M	A	Q4_OUT	Q4_OUT
PLL_ON_OFF_TEMP	Output	PS02M	A	PLL_ON_OFF	PLL_ON_OFF
OCIA_EN_TEMP	Output	PS02M	A	OCIA_EN	OCIA_EN
USB_SUSPEND_TEMP	Output	PS02M	A	USB_SUSPEND	USB_SUSPEND
BGTRIM_TEMP_8	Output	PS02M	A	BGTRIM(8)	BGTRIM(8)
BGTRIM_TEMP_7	Output	PS02M	A	BGTRIM(7)	BGTRIM(7)
BGTRIM_TEMP_6	Output	PS02M	A	BGTRIM(6)	BGTRIM(6)
BGTRIM_TEMP_5	Output	PS02M	A	BGTRIM(5)	BGTRIM(5)
BGTRIM_TEMP_4	Output	PS02M	A	BGTRIM(4)	BGTRIM(4)
BGTRIM_TEMP_3	Output	PS02M	A	BGTRIM(3)	BGTRIM(3)

BGTRIM_TEMP_2	Output	PS02M	A	BGTRIM(2)	BGTRIM(2)
BGTRIM_TEMP_1	Output	PS02M	A	BGTRIM(1)	BGTRIM(1)
BGTRIM_TEMP_0	Output	PS02M	A	BGTRIM(0)	BGTRIM(0)

Signal to/from Multicore	Production	ICE	Tie offs for Production	Notes
SCAN_STAND	Used	Used		
EMU_WDT_INH	Not-used	Used	0	
EMULATE_EN	Not-used	Used	0	
TEST_EN	Used	Used		
FLASH_WR_EN	Used	Used		
RESET	Used	Used		
A0_IN	Used	Used		
ALE_IN	Used	Used		
CS	Used	Used		
WR	Used	Used		
RD	Used	Used		
TXD_BYPASS	Used	Used		
EMU_P13_IN	Not-used	Used	0	
PORT3_OUT(3) DMA_ACK_EN DMA_ACK_SDCI_CLK_IN	Used	Used		
DMA_REQUEST DMA_REQ_EN P15_IN	Used	Used		

CPU_PSEN	Not-used	Used	
EMULATE_EN_N			
EMU_PSEN			1
MEM_ALE	Not-used	Used	
EMULATE_EN_N			
EMU_ALE			0
CPU_RD	Not-used	Used	
EMULATE_EN_N			
EMU_MEMR			1
CPU_WR	Not-used	Used	
EMULATE_EN_N			
EMU_MEMW			1
AD_A(0)	Not-used	Used	
AD_EN			
EMU_AD_IN(0)			0
AD_A(1)	Not-used	Used	
AD_EN			
EMU_AD_IN(1)			0
AD_A(2)	Not-used	Used	
AD_EN			
EMU_AD_IN(2)			0
AD_A(3)	Not-used	Used	
AD_EN			
EMU_AD_IN(3)			0
AD_A(4)	Not-used	Used	
AD_EN			
EMU_AD_IN(4)			0

AD_A(5) AD_EN EMU_AD_IN(5)	Not-used	Used	0
AD_A(6) AD_EN EMU_AD_IN(6)	Not-used	Used	0
AD_A(7) AD_EN EMU_AD_IN(7)	Not-used	Used	0
CPU_ADDR(8) EMULATE_EN_N EMU_ADDR_IN(8)	Not-used	Used	0
CPU_ADDR(9) EMULATE_EN_N EMU_ADDR_IN(9)	Not-used	Used	0
CPU_ADDR(10) EMULATE_EN_N EMU_ADDR_IN(10)	Not-used	Used	0
CPU_ADDR(11) EMULATE_EN_N EMU_ADDR_IN(11)	Not-used	Used	0
CPU_ADDR(12) EMULATE_EN_N EMU_ADDR_IN(12)	Not-used	Used	0
CPU_ADDR(13) EMULATE_EN_N EMU_ADDR_IN(13)	Not-used	Used	0
CPU_ADDR(14)	Not-used	Used	

EMULATE_EN_N EMU_ADDR_IN(14)			0
CPU_ADDR(15) EMULATE_EN_N EMU_ADDR_IN(15)	Not-used	Used	0
PORT1_OUT(1) EMULATE_EN_N EMU_P11_IN	Not-used	Used	0
PORT1_OUT(6) EMULATE_EN_N EMU_P16_IN	Not-used	Used	0
PORT3_OUT(1) EMULATE_EN_N EMU_P31_IN	Not-used	Used	0
D_OUT(0) D_OUT_EN D_IN(0)	Used	Used	
D_OUT(1) D_OUT_EN D_IN(1)	Used	Used	
D_OUT(2) D_OUT_EN D_IN(2)	Used	Used	
D_OUT(3) D_OUT_EN D_IN(3)	Used	Used	
D_OUT(4) D_OUT_EN	Used	Used	

D_IN(4)		
D_OUT(5) D_OUT_EN D_IN(5)	Used	Used
D_OUT(6) D_OUT_EN D_IN(6)	Used	Used
D_OUT(7) D_OUT_EN D_IN(7)	Used	Used
PORT1_OUT(3) RSV1_EN P13_IN	Used	Used
PORT1_OUT(2) RSV2_EN P12_IN	Used	Used
SUSPEND_TEMP	Used	Used
EXT_WAKEUP	Used	Used
INT	Used	Used
EOT	Used	Used
DEC_CLKOUT	Used	Used
RXD_BYPASS	Used	Used
BAUD_CLK	Not-used	Used
P12_OUT	Not-used	Used

P14_IN	Not-used	Used		
PORT1_OUT(5)	Not-used	Used		
P17_IN	Not-used	Used		
PORT3_IN(0)	Not-used	Used		
PORT3_IN(2)	Not-used	Used		
PORT3_IN(3)	Not-used	Used		
PORT3_IN(4)	Not-used	Used		
PORT3_IN(5)	Not-used	Used		
SOF_TOGGLE	Used	Used		
	Used	Used		From Analog IO
CPU_OSC	Not_used	Used		

Signal to/from Multicore	**Production**	**ICE**	**Tie off for Production**	**Notes**
DIP	Used	Used		
DIM	Used	Used		
B1_IN	Used	Used		
DIDIF	Used	Used		
OCIA_CLKOUT	Used	Used		

B2_IN	Used	Used
B3_IN	Used	Used
OCIA_CLKIN	Used	Used
OCIA_SDATA	Used	Used
N_DOWNLOAD	Used	Used
RS232_IN2	Used	Used
RS232_IN1	Used	Used
FCLK_TEMP	Used	Used
N_TG_EN	Used	Used
RES_IN	Used	Used
DOP	Used	Used
DOM	Used	Used
NDOE	Used	Used
Q5_OUT	Used	Used
N_RS232_TEN	Used	Used
RS232_OUT1	Used	Used
RS232_OUT2	Used	Used
CP_ON	Used	Used

RS485_OE	Used	Used
SYN_EN	Used	Used
KBD_WAND_EN	Used	Used
N_RS232_REN	Used	Used
USB_CONN	Used	Used
KBD_CLOSE	Used	Used
Q1_OUT	Used	Used
Q2_OUT	Used	Used
Q3_OUT	Used	Used
Q4_OUT	Used	Used
PLL_ON_OFF	Used	Used
OCIA_EN	Used	Used
USB_SUSPEND	Used	Used
BGTRIM(8)	Used	Used
BGTRIM(7)	Used	Used
BGTRIM(6)	Used	Used
BGTRIM(5)	Used	Used
BGTRIM(4)	Used	Used
BGTRIM(3)	Used	Used

BGTRIM(2)	Used	Used
BGTRIM(1)	Used	Used
BGTRIM(0)	Used	Used

EXHIBIT O

Label > AD	A	ALE	WR	RD	INT2	Descriptio
321	1	98	0	1	1	0
322	1	98	0	1	0	0
323	8	98	0	1	0	0
324	8	98	0	1	0	0
325	8	98	0	1	0	0
326	8	98	0	1	1	0
327	16	98	1	1	1	0
328 FF		42	0	1	1	0
329	8	98	0	1	1	0
330	8	98	0	1	1	0
331	8	98	0	1	0	0
332	8	98	0	1	0	0
333	80	98	0	1	0	0
334	80	98	0	1	0	0
335	80	98	0	1	1	0
336	20	98	1	1	1	0
337 FF		42	0	1	1	0
338	80	98	0	1	1	0
339	80	98	0	1	1	0
340	80	98	0	1	0	0
341	80	98	0	1	0	0
342	6	98	0	1	0	0
343	6	98	0	1	0	0
344	6	98	0	1	1	0
345	20	98	1	1	1	0
346 FF		42	0	1	1	0
347	6	98	0	1	1	0
348	6	98	0	1	1	0
349	6	98	0	1	0	0
350	6	98	0	1	0	0
351	0	98	0	1	0	0
352	0	98	0	1	0	0
353	0	98	0	1	1	0
354	20	98	1	1	1	0
355 FF		42	0	1	1	0
356	0	98	0	1	1	0
357	0	98	0	1	1	0
358	0	98	0	1	0	0
359	0	98	0	1	0	0
360	1	98	0	1	0	0
361	1	98	0	1	0	0
362	1	98	0	1	1	0
363	20	98	1	1	1	0
364 FF		42	0	1	1	0
365	1	98	0	1	1	0

366	1	98	0	1	1	0
367	1	98	0	1	0	0
368	1	98	0	1	0	0
369	0	98	0	1	0	0
370	0	98	0	1	0	0
371	0	98	0	1	1	0
372	20	98	1	1	1	0
373 FF		42	0	1	1	0
374	0	98	0	1	1	0
375	0	98	0	1	1	0
376	0	98	0	1	0	0
377	0	98	0	1	0	0
378	0	98	0	1	0	0
379	0	98	0	1	0	0
380	0	98	0	1	1	0
381	20	98	1	1	1	0
382 FF		42	0	1	1	0
383	0	98	0	1	1	0
384	0	98	0	1	1	0
385	0	98	0	1	0	0
386	0	98	0	1	0	0
387	40	98	0	1	0	0
388	40	98	0	1	0	0
389	40	98	0	1	1	0
390	20	98	1	1	1	0
391 FF		42	0	1	1	0
392	40	98	0	1	1	0
393	40	98	0	1	1	0
394	40	98	0	1	0	0
395	40	98	0	1	0	0
396	0	98	0	1	0	0
397	0	98	0	1	0	0
398	0	98	0	1	1	0
399	20	98	1	1	1	0
400 FF		42	0	1	1	0
401	0	98	0	1	1	0
402	0	98	0	1	1	0
403	40	98	0	0	1	0
404	40	98	0	0	1	0
405	40	98	0	0	1	0
406	40	98	0	0	1	0
407	0	98	0	1	1	0
408	11	98	1	1	1	0
409 FF		42	0	1	1	0
410	0	98	0	1	1	0
411	0	98	0	1	1	0
412	12	98	0	0	1	0
413	12	98	0	0	1	0
414	12	98	0	0	1	0
415	12	98	0	0	1	0
416	0	98	0	1	1	0
417	20	98	1	1	1	0

418 FF		48	0	1	1	0
419	0	98	0	1	1	0
420	0	98	0	1	1	0
421	1	98	0	0	1	0
422	1	98	0	0	1	0
423	1	98	0	0	1	0
424	1	98	0	0	1	0
425	0	98	0	1	1	0
426	20	98	1	1	1	0
427 FF		48	0	1	1	0
428	0	98	0	1	1	0
429	0	98	0	1	1	0
430	10	98	0	0	1	0
431	10	98	0	0	1	0
432	10	98	0	0	1	0
433	10	98	0	0	1	0
434	0	98	0	1	1	0
435	20	98	1	1	1	0
436 FF		48	0	1	1	0
437	0	98	0	1	1	0
438	0	98	0	1	1	0
439	1	98	0	0	1	0
440	1	98	0	0	1	0
441	1	98	0	0	1	0
442	1	98	0	0	1	0
443	0	98	0	1	1	0
444	20	98	1	1	1	0
445 FF		48	0	1	1	0
446	0	98	0	1	1	0
447	0	98	0	1	1	0
448	0	98	0	0	1	0
449	0	98	0	0	1	0
450	0	98	0	0	1	0
451	0	98	0	0	1	0
452	0	98	0	1	1	0
453	20	98	1	1	1	0
454 FF		48	0	1	1	0
455	0	98	0	1	1	0
456	0	98	0	1	1	0
457	0	98	0	0	1	0
458	0	98	0	0	1	0
459	0	98	0	0	1	0
460	0	98	0	0	1	0
461	0	98	0	1	1	0
462	20	98	1	1	1	0
463 FF		48	0	1	1	0
464	0	98	0	1	1	0
465	0	98	0	1	1	0
466	0	98	0	0	1	0
467	0	98	0	0	1	0
468	0	98	0	0	1	0
469	0	98	0	0	1	0

470	0	98	0	1	1	0	
471	20	98	1	1	1	0	
472 FF		48	0	1	1	0	
473	0	98	0	1	1	0	
474	0	98	0	1	1	0	
475	8	98	0	0	1	0	
476	8	98	0	0	1	0	
477	8	98	0	0	1	0	
478	8	98	0	0	1	0	
479	0	98	0	1	1	0	
480	20	98	1	1	1	0	
481 FF		48	0	1	1	0	
482	0	98	0	1	1	0	
483	0	98	0	1	1	0	
484	2	98	0	0	1	0	
485	2	98	0	0	1	0	
486	2	98	0	0	1	0	
487	2	98	0	0	1	0	
488	0	98	0	1	1	0	
489	11	98	1	1	1	0	
490 FF		48	0	1	1	0	
491 FF	2C		0	1	1	1	*First usb i*
492 2F	2C		1	1	1	1	
493	0	91	0	1	1	1	
494	0	91	0	1	1	1	
495	0	91	0	1	1	1	
496	0	91	0	1	0	0	
497	0	98	0	1	1	0	
498	0	98	0	1	1	0	
499	0	98	0	1	0	0	
500	0	98	0	1	0	0	
501	0	98	0	1	0	0	
502	0	98	0	1	0	0	
503	0	98	0	1	1	0	
504	6	98	1	1	1	0	*Read INTR*
505 FF		50	0	1	1	0	
506	0	98	0	1	1	0	
507	0	98	0	1	1	0	
508	0	98	0	1	0	0	
509	1	98	0	1	0	0	
510	1	98	0	1	0	0	
511	1	98	0	1	0	0	
512	1	98	0	1	1	0	
513	2	98	1	1	1	0	*Read INTR*
514 FF		50	0	1	1	0	
515	1	98	0	1	1	0	
516	1	98	0	1	1	0	
517	1	98	0	1	0	0	
518	0	98	0	1	0	0	
519	0	98	0	1	0	0	
520	0	98	0	1	0	0	
521	0	98	0	1	1	0	

522	3	98	1	1	1	0	*Read INTR*
523 FF		50	0	1	1	0	
524	0	98	0	1	1	0	
525	0	98	0	1	1	0	
526	0	98	0	1	0	0	
527	0	98	0	1	0	0	
528	0	98	0	1	0	0	
529	0	98	0	1	0	0	
530	0	98	0	1	1	0	
531	4	98	1	1	1	0	*Read INTR*
532 FF		50	0	1	1	0	
533	0	98	0	1	1	0	
534	0	98	0	1	1	0	
535	0	98	0	1	0	0	
536	0	98	0	1	0	0	
537	0	98	0	1	0	0	
538	0	98	0	1	0	0	
539	0	98	0	1	1	0	
540	5	98	1	1	1	0	*Read INTR*
541 FF		50	0	1	1	0	
542	42	50	0	1	1	1	*2nd USB i*
543	42	50	0	1	1	1	
544 6C		50	1	1	1	1	
545	42	50	0	1	1	1	
546	0	98	0	1	1	0	
547	0	98	0	1	1	0	
548	0	98	0	1	0	0	
549	10	98	0	1	0	0	
550	10	98	0	1	0	0	
551	10	98	0	1	0	0	
552	10	98	0	1	1	0	
553	11	98	1	1	1	0	*Read CSR*
554 FF	4B		0	1	1	0	
555	10	98	0	1	1	0	
556	10	98	0	1	1	0	
557	10	98	0	1	0	0	
558	0	98	0	1	0	0	
559	0	98	0	1	0	0	
560	0	98	0	1	0	0	
561	0	98	0	1	1	0	
562	1	98	1	1	1	0	*Read Pow*
563 FF	4B		0	1	1	0	
564	0	98	0	1	1	0	
565	0	98	0	1	1	0	
566	1	98	0	0	1	0	
567	1	98	0	0	1	0	
568	1	98	0	0	1	0	
569	1	98	0	0	1	0	
570	0	98	0	1	1	0	
571	1	98	1	1	1	0	*Write Pow*
572 FF	4B		0	1	1	0	
573	0	98	0	1	1	0	

574	0	98	0	1	1	0	
575	0	98	0	1	0	0	
576	0	98	0	1	0	0	
577	0	98	0	1	0	0	
578	0	98	0	1	0	0	
579	0	98	0	1	1	0	
580	0E	98	1	1	1	0	*Read Inde*
581	FF 4B		0	1	1	0	
582	0	98	0	1	1	0	
583	0	98	0	1	1	0	
584	0	98	0	0	1	0	
585	0	98	0	0	1	0	
586	0	98	0	0	1	0	
587	0	98	0	0	1	0	
588	0	98	0	1	1	0	
589	0E	98	1	1	1	0	*Write Inde*
590	FF 4B		0	1	1	0	
591	0	98	0	1	1	0	
592	0	98	0	1	1	0	
593	0	98	0	1	0	0	
594	10	98	0	1	0	0	
595	10	98	0	1	0	0	
596	10	98	0	1	0	0	
597	10	98	0	1	1	0	
598	11	98	1	1	1	0	*Read CSR*
599	FF 4C		0	1	1	0	
600	10	98	0	1	1	0	
601	10	98	0	1	1	0	
602	10	98	0	1	0	0	
603	10	98	0	1	0	0	
604	10	98	0	1	0	0	
605	10	98	0	1	0	0	
606	10	98	0	1	1	0	
607	11	98	1	1	1	0	*Read CSR*
608	FF 4C		0	1	1	0	
609	10	98	0	1	1	0	
610	10	98	0	1	1	0	
611	90	98	0	0	1	0	
612	90	98	0	0	1	0	
613	90	98	0	0	1	0	
614	90	98	0	0	1	0	
615	10	98	0	1	1	0	
616	11	98	1	1	1	0	*Write CSR*
617	FF 4C		0	1	1	0	
618	10	98	0	1	1	0	
619	10	98	0	1	1	0	
620	10	98	0	1	0	0	
621	0	98	0	1	0	0	
622	0	98	0	1	0	0	
623	0	98	0	1	0	0	
624	0	98	0	1	1	0	
625	11	98	1	1	1	0	*Read CSR*

626	FF		42	0	1	1	0	
627		0	98	0	1	1	0	
628		0	98	0	1	1	0	
629		0	98	0	1	0	0	
630		0	98	0	1	0	0	
631		0	98	0	1	0	0	
632		0	98	0	1	0	0	
633		0	98	0	1	1	0	
634		6	98	1	1	1	0	***Read INTR***
635	FF		50	0	1	1	0	
636		0	98	0	1	1	0	
637		0	98	0	1	1	0	
638		0	98	0	1	0	0	
639		1	98	0	1	0	0	
640		1	98	0	1	0	0	
641		1	98	0	1	0	0	
642		1	98	0	1	1	0	
643		2	98	1	1	1	0	***Read INTR***
644	FF		50	0	1	1	0	
645		1	98	0	1	1	0	
646		1	98	0	1	1	0	
647		1	98	0	1	0	0	
648		0	98	0	1	0	0	
649		0	98	0	1	0	0	
650		0	98	0	1	0	0	
651		0	98	0	1	1	0	
652		3	98	1	1	1	0	***Read INTR***
653	FF		50	0	1	1	0	
654		0	98	0	1	1	0	
655		0	98	0	1	1	0	
656		0	98	0	1	0	0	
657		0	98	0	1	0	0	
658		0	98	0	1	0	0	
659		0	98	0	1	0	0	
660		0	98	0	1	1	0	
661		4	98	1	1	1	0	***Read INTR***
662	FF		50	0	1	1	0	
663		0	98	0	1	1	0	
664		0	98	0	1	1	0	
665		0	98	0	1	0	0	
666		0	98	0	1	0	0	
667		0	98	0	1	0	0	
668		0	98	0	1	0	0	
669		0	98	0	1	1	0	
670		5	98	1	1	1	0	***Read INTR***
671	FF		50	0	1	1	0	
672		0	98	0	1	1	0	
673		0	98	0	1	1	0	
674		0	98	0	1	0	0	
675		0	98	0	1	0	0	
676		0	98	0	1	0	0	
677		0	98	0	1	0	0	

678	0	98	0	1	1	0	
679	11	98	**1**	1	1	0	***Read CSR***
680 FF	4B		0	1	1	0	
681	0	98	0	1	1	0	
682	0	98	0	1	1	0	
683	0	98	0	1	0	0	
684	1	98	0	1	0	0	
685	1	98	0	1	0	0	
686	1	98	0	1	0	0	
687	1	98	0	1	1	0	
688	1	98	**1**	1	1	0	***Read Pow***
689 FF	4B		0	1	1	0	
690	1	98	0	1	1	0	
691	1	98	0	1	1	0	
692	1	98	0	1	0	0	
693	0	98	0	1	0	0	
694	0	98	0	1	0	0	
695	0	98	0	1	0	0	
696	0	98	0	1	1	0	
697 0E		98	**1**	1	1	0	***Read Inde***
698 FF	4B		0	1	1	0	
699	0	98	0	1	1	0	
700	0	98	0	1	1	0	
701	0	98	0	0	1	0	
702	0	98	0	0	1	0	
703	0	98	0	0	1	0	
704	0	98	0	0	1	0	
705	0	98	0	1	1	0	
706 0E		98	**1**	1	1	0	***Write Inde***
707 FF	4B		0	1	1	0	
708	0	98	0	1	1	0	
709	0	98	0	1	1	0	
710	0	98	0	1	0	0	
711	0	98	0	1	0	0	
712	0	98	0	1	0	0	
713	0	98	0	1	0	0	
714	0	98	0	1	1	0	
715	11	98	**1**	1	1	0	***Read CSR***
716 FF	4C		0	1	1	0	
717	0	98	0	1	1	0	
718	0	98	0	1	1	0	
719	0	98	0	1	0	0	
720	0	98	0	1	0	0	
721	0	98	0	1	0	0	
722	0	98	0	1	0	0	
723	0	98	0	1	1	0	
724	11	98	**1**	1	1	0	***Read CSR***
725 FF	4C		0	1	1	0	
726	0	98	0	1	1	0	
727	0	98	0	1	1	0	
728	0	98	0	1	0	0	
729	0	98	0	1	0	0	

730	0	98	0	1	0	0	
731	0	98	0	1	0	0	
732	0	98	0	1	1	0	
733	11	98	1	1	1	0	*Read CSR*
734 FF		42	0	1	1	0	
735 E0		68	0	1	1	1	*3rd USB Ir*
736 E0		68	0	1	1	1	
737	66	68	1	1	1	1	
738 E0		68	0	1	1	1	
739	0	98	0	1	1	0	
740	0	98	0	1	1	0	
741	0	98	0	1	0	0	
742	4	98	0	1	0	0	
743	4	98	0	1	0	0	
744	4	98	0	1	0	0	
745	4	98	0	1	1	0	
746	6	98	1	1	1	0	*Read INTU*
747 FF		50	0	1	1	0	
748	4	98	0	1	1	0	
749	4	98	0	1	1	0	
750	4	98	0	1	0	0	
751	0	98	0	1	0	0	
752	0	98	0	1	0	0	
753	0	98	0	1	0	0	
754	0	98	0	1	1	0	
755	2	98	1	1	1	0	*Read INTR*
756 FF		50	0	1	1	0	
757	0	98	0	1	1	0	
758	0	98	0	1	1	0	
759	0	98	0	1	0	0	
760	0	98	0	1	0	0	
761	0	98	0	1	0	0	
762	0	98	0	1	0	0	
763	0	98	0	1	1	0	
764	3	98	1	1	1	0	*Read INTR*
765 FF		50	0	1	1	0	
766	0	98	0	1	1	0	
767	0	98	0	1	1	0	
768	0	98	0	1	0	0	
769	0	98	0	1	0	0	
770	0	98	0	1	0	0	
771	0	98	0	1	0	0	
772	0	98	0	1	1	0	
773	4	98	1	1	1	0	*Read INTR*
774 FF		50	0	1	1	0	
775	0	98	0	1	1	0	
776	0	98	0	1	1	0	
777	0	98	0	1	0	0	
778	0	98	0	1	0	0	
779	0	98	0	1	0	0	
780	0	98	0	1	0	0	
781	0	98	0	1	1	0	

782	5	98	1	1	1	0	*Read INTR*
783 FF		50	0	1	1	0	
784	0	98	0	1	1	0	
785	0	98	0	1	1	0	
786	0	98	0	1	0	0	
787	0	98	0	1	0	0	
788	0	98	0	1	0	0	
789	0	98	0	1	0	0	
790	0	98	0	1	1	0	
791	0	98	1	1	1	0	*Read FAD*
792 FF		46	0	1	1	0	
793	0	98	0	1	1	0	
794	0	98	0	1	1	0	
795	0	98	0	0	1	0	
796	0	98	0	0	1	0	
797	0	98	0	0	1	0	
798	0	98	0	0	1	0	
799	0	98	0	1	1	0	
800	0	98	1	1	1	0	*Write FAD*
801 FF		46	0	1	1	0	
802	0	98	0	1	1	0	
803	0	98	0	1	1	0	
804	0	98	0	0	1	0	
805	0	98	0	0	1	0	
806	0	98	0	0	1	0	
807	0	98	0	0	1	0	
808	0	98	0	1	1	0	
809	7	98	1	1	1	0	*Write INTR*
810 FF		46	0	1	1	0	
811	0	98	0	1	1	0	
812	0	98	0	1	1	0	
813	0	98	0	0	1	0	
814	0	98	0	0	1	0	
815	0	98	0	0	1	0	
816	0	98	0	0	1	0	
817	0	98	0	1	1	0	
818	8	98	1	1	1	0	*Write INTR*
819 FF		46	0	1	1	0	
820	0	98	0	1	1	0	
821	0	98	0	1	1	0	
822	0	98	0	0	1	0	
823	0	98	0	0	1	0	
824	0	98	0	0	1	0	
825	0	98	0	0	1	0	
826	0	98	0	1	1	0	
827	9	98	1	1	1	0	*Write INTR*
828 FF		46	0	1	1	0	
829	0	98	0	1	1	0	
830	0	98	0	1	1	0	
831	0	98	0	0	1	0	
832	0	98	0	0	1	0	
833	0	98	0	0	1	0	

834	0	98	0	0	1	0	
835	0	98	0	1	1	0	
836	0A	98	1	1	1	0	*Write INTR*
837	FF	46	0	1	1	0	
838	0	98	0	1	1	0	
839	0	98	0	1	1	0	
840	0	98	0	1	0	0	
841	0	98	0	1	0	0	
842	0	98	0	1	0	0	
843	0	98	0	1	0	0	
844	0	98	0	1	1	0	
845	7	98	1	1	1	0	*Read INTR*
846	FF	6E	0	1	1	0	
847	0	98	0	1	1	0	
848	0	98	0	1	1	0	
849	1	98	0	0	1	0	
850	1	98	0	0	1	0	
851	1	98	0	0	1	0	
852	1	98	0	0	1	0	
853	0	98	0	1	1	0	
854	7	98	1	1	1	0	*Write INTR*
855	FF	6E	0	1	1	0	
856	0	98	0	1	1	0	
857	0	98	0	1	1	0	
858	7	98	0	0	1	0	
859	7	98	0	0	1	0	
860	7	98	0	0	1	0	
861	7	98	0	0	1	0	
862	0	98	0	1	1	0	
863	0B	98	1	1	1	0	*Write INTL*
864	FF	6E	0	1	1	0	
865	64	21	0	1	1	1	*4th USB in*
866	7	21	1	1	1	1	
867	64	3E	0	1	1	1	
868	BB	3E	0	1	1	1	
869	0	98	0	1	1	0	
870	0	98	0	1	1	0	
871	0	98	0	1	0	0	
872	0	98	0	1	0	0	
873	0	98	0	1	0	0	
874	0	98	0	1	0	0	
875	0	98	0	1	1	0	
876	6	98	1	1	1	0	*Read INTR*
877	FF	50	0	1	1	0	
878	0	98	0	1	1	0	
879	0	98	0	1	1	0	
880	0	98	0	1	0	0	
881	1	98	0	1	0	0	
882	1	98	0	1	0	0	
883	1	98	0	1	0	0	
884	1	98	0	1	1	0	
885	2	98	1	1	1	0	*Read INTR*

886	FF		50	0	1	1	0	
887		1	98	0	1	1	0	
888		1	98	0	1	1	0	
889		1	98	0	1	0	0	
890		0	98	0	1	0	0	
891		0	98	0	1	0	0	
892		0	98	0	1	0	0	
893		0	98	0	1	1	0	
894		3	98	1	1	1	0	***Read INTR***
895	FF		50	0	1	1	0	
896		0	98	0	1	1	0	
897		0	98	0	1	1	0	
898		0	98	0	1	0	0	
899		0	98	0	1	0	0	
900		0	98	0	1	0	0	
901		0	98	0	1	0	0	
902		0	98	0	1	1	0	
903		4	98	1	1	1	0	***Read INTR***
904	FF		50	0	1	1	0	
905		0	98	0	1	1	0	
906		0	98	0	1	1	0	
907		0	98	0	1	0	0	
908		0	98	0	1	0	0	
909		0	98	0	1	0	0	
910		0	98	0	1	0	0	
911		0	98	0	1	1	0	
912		5	98	1	1	1	0	***Read INTR***
913	FF		50	0	1	1	0	
914		0	98	0	1	1	0	
915		0	98	0	1	1	0	
916		0	98	0	1	0	0	
917		1	98	0	1	0	0	
918		1	98	0	1	0	0	
919		1	98	0	1	0	0	
920		1	98	0	1	1	0	
921		11	98	1	1	1	0	***Read CSR***
922	FF	4B		0	1	1	0	
923		1	98	0	1	1	0	
924		1	98	0	1	1	0	
925		1	98	0	1	0	0	
926		0	98	0	1	0	0	
927		0	98	0	1	0	0	
928		0	98	0	1	0	0	
929		0	98	0	1	1	0	
930	0E		98	1	1	1	0	***Read Inde***
931	FF	4B		0	1	1	0	
932		0	98	0	1	1	0	
933		0	98	0	1	1	0	
934		0	98	0	0	1	0	
935		0	98	0	0	1	0	
936		0	98	0	0	1	0	
937		0	98	0	0	1	0	

938	0	98	0	1	1	0	
939 0E		98	1	1	1	0	*Write Inde*
940 FF	4B		0	1	1	0	
941	0	98	0	1	1	0	
942	0	98	0	1	1	0	
943	0	98	0	1	0	0	
944	1	98	0	1	0	0	
945	1	98	0	1	0	0	
946	1	98	0	1	0	0	
947	1	98	0	1	1	0	
948	11	98	1	1	1	0	*Read CSR*
949 FF	4C		0	1	1	0	
950	1	98	0	1	1	0	
951	1	98	0	1	1	0	
952	1	98	0	1	0	0	
953	1	98	0	1	0	0	
954	1	98	0	1	0	0	
955	1	98	0	1	0	0	
956	1	98	0	1	1	0	
957	11	98	1	1	1	0	*Read CSR*
958 FF	4C		0	1	1	0	
959	1	98	0	1	1	0	
960	1	98	0	1	1	0	
961	1	98	0	1	0	0	
962	1	98	0	1	0	0	
963	1	98	0	1	0	0	
964	1	98	0	1	0	0	
965	1	98	0	1	1	0	
966	11	98	1	1	1	0	*Read CSR*
967 FF		42	0	1	1	0	
968	1	98	0	1	1	0	
969	1	98	0	1	1	0	
970	1	98	0	1	0	0	
971	8	98	0	1	0	0	
972	8	98	0	1	0	0	
973	8	98	0	1	0	0	
974	8	98	0	1	1	0	
975	16	98	1	1	1	0	*Read Cou*
976 FF		42	0	1	1	0	
977	8	98	0	1	1	0	
978	8	98	0	1	1	0	
979	8	98	0	1	0	0	
980	8	98	0	1	0	0	
981	0	98	0	1	0	0	
982	0	98	0	1	0	0	
983	0	98	0	1	1	0	
984	20	98	1	1	1	0	*Read Fifo,*
985 FF		42	0	1	1	0	
986	0	98	0	1	1	0	
987	0	98	0	1	1	0	
988	0	98	0	1	0	0	
989	0	98	0	1	0	0	

990	5	98	0	1	0	0	
991	5	98	0	1	0	0	
992	5	98	0	1	1	0	
993	20	98	1	1	1	0	***Read Fifo,***
994 FF		42	0	1	1	0	
995	5	98	0	1	1	0	
996	5	98	0	1	1	0	
997	5	98	0	1	0	0	
998	5	98	0	1	0	0	
999	2	98	0	1	0	0	
1000	2	98	0	1	0	0	
1001	2	98	0	1	1	0	
1002	20	98	1	1	1	0	***Read Fifo,***
1003 FF		42	0	1	1	0	
1004	2	98	0	1	1	0	
1005	2	98	0	1	1	0	
1006	2	98	0	1	0	0	
1007	2	98	0	1	0	0	
1008	0	98	0	1	0	0	
1009	0	98	0	1	0	0	
1010	0	98	0	1	1	0	
1011	20	98	1	1	1	0	***Read Fifo,***
1012 FF		42	0	1	1	0	
1013	0	98	0	1	1	0	
1014	0	98	0	1	1	0	
1015	0	98	0	1	0	0	
1016	0	98	0	1	0	0	
1017	0	98	0	1	0	0	
1018	0	98	0	1	0	0	
1019	0	98	0	1	1	0	
1020	20	98	1	1	1	0	***Read Fifo,***
1021 FF		42	0	1	1	0	
1022	0	98	0	1	1	0	
1023	0	98	0	1	1	0	
1024	0	98	0	1	0	0	
1025	0	98	0	1	0	0	
1026	0	98	0	1	0	0	
1027	0	98	0	1	0	0	
1028	0	98	0	1	1	0	
1029	20	98	1	1	1	0	***Read Fifo,***
1030 FF		42	0	1	1	0	
1031	0	98	0	1	1	0	
1032	0	98	0	1	1	0	
1033	0	98	0	1	0	0	
1034	0	98	0	1	0	0	
1035	0	98	0	1	0	0	
1036	0	98	0	1	0	0	
1037	0	98	0	1	1	0	
1038	20	98	1	1	1	0	***Read Fifo,***
1039 FF		42	0	1	1	0	
1040	0	98	0	1	1	0	
1041	0	98	0	1	1	0	

1042	0	98	0	1	0	0	
1043	0	98	0	1	0	0	
1044	0	98	0	1	0	0	
1045	0	98	0	1	0	0	
1046	0	98	0	1	1	0	
1047	20	98	1	1	1	0	*Read Fifo,*
1048 FF		42	0	1	1	0	
1049	0	98	0	1	1	0	
1050	0	98	0	1	1	0	
1051	48	98	0	0	1	0	
1052	48	98	0	0	1	0	
1053	48	98	0	0	1	0	
1054	48	98	0	0	1	0	
1055	0	98	0	1	1	0	
1056	11	98	1	1	1	0	*Write CSR*
1057 FF		42	0	1	1	0	
1058 D0		50	0	1	1	1	*5th USB in*
1059 B1		50	1	1	1	1	
1060 D0		50	0	1	1	1	
1061 FF	5F		0	1	1	1	
1062	0	50	0	1	1	1	
1063	0	50	0	1	1	0	
1064	0	98	0	1	1	0	
1065	0	98	0	1	1	0	
1066	0	98	0	1	0	0	
1067	0	98	0	1	0	0	
1068	0	98	0	1	0	0	
1069	0	98	0	1	0	0	
1070	0	98	0	1	1	0	
1071	6	98	1	1	1	0	*Read INTR*
1072 FF		50	0	1	1	0	
1073	0	98	0	1	1	0	
1074	0	98	0	1	1	0	
1075	0	98	0	1	0	0	
1076	1	98	0	1	0	0	
1077	1	98	0	1	0	0	
1078	1	98	0	1	0	0	
1079	1	98	0	1	1	0	
1080	2	98	1	1	1	0	*Read INTR*
1081 FF		50	0	1	1	0	
1082	1	98	0	1	1	0	
1083	1	98	0	1	1	0	
1084	1	98	0	1	0	0	
1085	0	98	0	1	0	0	
1086	0	98	0	1	0	0	
1087	0	98	0	1	0	0	
1088	0	98	0	1	1	0	
1089	3	98	1	1	1	0	*Read INTR*
1090 FF		50	0	1	1	0	
1091	0	98	0	1	1	0	
1092	0	98	0	1	1	0	
1093	0	98	0	1	0	0	

1094	0	98	0	1	0	0	
1095	0	98	0	1	0	0	
1096	0	98	0	1	0	0	
1097	0	98	0	1	1	0	
1098	4	98	1	1	1	0	*Read INTR*
1099 FF		50	0	1	1	0	
1100	0	98	0	1	1	0	
1101	0	98	0	1	1	0	
1102	0	98	0	1	0	0	
1103	0	98	0	1	0	0	
1104	0	98	0	1	0	0	
1105	0	98	0	1	0	0	
1106	0	98	0	1	1	0	
1107	5	98	1	1	1	0	*Read INTR*
1108 FF		50	0	1	1	0	
1109	0	98	0	1	1	0	
1110	0	98	0	1	1	0	
1111	0	98	0	1	0	0	
1112	0	98	0	1	0	0	
1113	0	98	0	1	0	0	
1114	0	98	0	1	0	0	
1115	0	98	0	1	1	0	
1116	11	98	1	1	1	0	*Read CSR*
1117 FF	4B		0	1	1	0	
1118	0	98	0	1	1	0	
1119	0	98	0	1	1	0	
1120	0	98	0	1	0	0	
1121	0	98	0	1	0	0	
1122	0	98	0	1	0	0	
1123	0	98	0	1	0	0	
1124	0	98	0	1	1	0	
1125	1	98	1	1	1	0	*Read Pow*
1126 FF	4B		0	1	1	0	
1127	0	98	0	1	1	0	
1128	0	98	0	1	1	0	
1129	1	98	0	0	1	0	
1130	1	98	0	0	1	0	
1131	1	98	0	0	1	0	
1132	1	98	0	0	1	0	
1133	0	98	0	1	1	0	
1134	1	98	1	1	1	0	*Write Pow*
1135 FF	4B		0	1	1	0	
1136	0	98	0	1	1	0	
1137	0	98	0	1	1	0	
1138	0	98	0	1	0	0	
1139	0	98	0	1	0	0	
1140	0	98	0	1	0	0	
1141	0	98	0	1	0	0	
1142	0	98	0	1	1	0	
1143	0	98	1	1	1	0	*Read FAD*
1144 FF	4B		0	1	1	0	
1145	0	98	0	1	1	0	

1146	0	98	0	1	1	0	
1147	2	98	0	0	1	0	
1148	2	98	0	0	1	0	
1149	2	98	0	0	1	0	
1150	2	98	0	0	1	0	
1151	0	98	0	1	1	0	
1152	0	98	1	1	1	0	***Write***
1153 FF	4B		0	1	1	0	
1154	0	98	0	1	1	0	
1155	0	98	0	1	1	0	
1156	0	98	0	1	0	0	
1157	0	98	0	1	0	0	
1158	0	98	0	1	0	0	
1159	0	98	0	1	0	0	
1160	0	98	0	1	1	0	
1161 0E		98	1	1	1	0	***Read Inde***
1162 FF	4B		0	1	1	0	
1163	0	98	0	1	1	0	
1164	0	98	0	1	1	0	
1165	0	98	0	0	1	0	
1166	0	98	0	0	1	0	
1167	0	98	0	0	1	0	
1168	0	98	0	0	1	0	
1169	0	98	0	1	1	0	
1170 0E		98	1	1	1	0	***Write Inde***
1171 FF	4B		0	1	1	0	
1172	0	98	0	1	1	0	
1173	0	98	0	1	1	0	
1174	0	98	0	1	0	0	
1175	0	98	0	1	0	0	
1176	0	98	0	1	0	0	
1177	0	98	0	1	0	0	
1178	0	98	0	1	1	0	
1179	11	98	1	1	1	0	***Read CSR***
1180 FF	4C		0	1	1	0	
1181	0	98	0	1	1	0	
1182	0	98	0	1	1	0	
1183	0	98	0	1	0	0	
1184	0	98	0	1	0	0	
1185	0	98	0	1	0	0	
1186	0	98	0	1	0	0	
1187	0	98	0	1	1	0	
1188	11	98	1	1	1	0	***Read CSR***
1189 FF	4C		0	1	1	0	
1190	0	98	0	1	1	0	
1191	0	98	0	1	1	0	
1192	0	98	0	1	0	0	
1193	0	98	0	1	0	0	
1194	0	98	0	1	0	0	
1195	0	98	0	1	0	0	
1196	0	98	0	1	1	0	

1197		11	98	1	1	1	0	*Read CSR*
1198	FF		42	0	1	1	0	
1199	FF	7F		0	1	1	1	*6th USB in*
1200		1 3E		0	1	1	1	
1201		1 3E		0	1	1	1	
1202	E5	3E		1	1	1	1	
1203		1 3E		0	1	1	1	
1204	FF	7F		0	1	1	0	
1205		0	98	0	1	1	0	
1206		0	98	0	1	1	0	
1207		0	98	0	1	0	0	
1208		0	98	0	1	0	0	
1209		0	98	0	1	0	0	
1210		0	98	0	1	0	0	
1211		0	98	0	1	1	0	
1212		6	98	1	1	1	0	
1213	FF		50	0	1	1	0	
1214		0	98	0	1	1	0	
1215		0	98	0	1	1	0	
1216		0	98	0	1	0	0	
1217		1	98	0	1	0	0	
1218		1	98	0	1	0	0	
1219		1	98	0	1	0	0	
1220		1	98	0	1	1	0	
1221		2	98	1	1	1	0	*Read INTR*
1222	FF		50	0	1	1	0	
1223		1	98	0	1	1	0	
1224		1	98	0	1	1	0	
1225		1	98	0	1	0	0	
1226		0	98	0	1	0	0	
1227		0	98	0	1	0	0	
1228		0	98	0	1	0	0	
1229		0	98	0	1	1	0	
1230		3	98	1	1	1	0	
1231	FF		50	0	1	1	0	
1232		0	98	0	1	1	0	
1233		0	98	0	1	1	0	
1234		0	98	0	1	0	0	
1235		0	98	0	1	0	0	
1236		0	98	0	1	0	0	
1237		0	98	0	1	0	0	
1238		0	98	0	1	1	0	
1239		4	98	1	1	1	0	
1240	FF		50	0	1	1	0	
1241		0	98	0	1	1	0	
1242		0	98	0	1	1	0	
1243		0	98	0	1	0	0	
1244		0	98	0	1	0	0	
1245		0	98	0	1	0	0	
1246		0	98	0	1	0	0	
1247		0	98	0	1	1	0	
1248		5	98	1	1	1	0	

1249	FF		50	0	1	1	0	
1250		0	98	0	1	1	0	
1251		0	98	0	1	1	0	
1252		0	98	0	1	0	0	
1253		1	98	0	1	0	0	
1254		1	98	0	1	0	0	
1255		1	98	0	1	0	0	
1256		1	98	0	1	1	0	
1257		11	98	1	1	1	0	*Read CSR*
1258	FF		4B	0	1	1	0	
1259		1	98	0	1	1	0	
1260		1	98	0	1	1	0	
1261		1	98	0	1	0	0	
1262		0	98	0	1	0	0	
1263		0	98	0	1	0	0	
1264		0	98	0	1	0	0	
1265		0	98	0	1	1	0	
1266	0E		98	1	1	1	0	
1267	FF		4B	0	1	1	0	
1268		0	98	0	1	1	0	
1269		0	98	0	1	1	0	
1270		0	98	0	0	1	0	
1271		0	98	0	0	1	0	
1272		0	98	0	0	1	0	
1273		0	98	0	0	1	0	
1274		0	98	0	1	1	0	
1275	0E		98	1	1	1	0	*Write Inde*
1276	FF		4B	0	1	1	0	
1277		0	98	0	1	1	0	
1278		0	98	0	1	1	0	
1279		0	98	0	1	0	0	
1280		1	98	0	1	0	0	
1281		1	98	0	1	0	0	
1282		1	98	0	1	0	0	
1283		1	98	0	1	1	0	
1284		11	98	1	1	1	0	*Read CSR*
1285	FF		4C	0	1	1	0	
1286		1	98	0	1	1	0	
1287		1	98	0	1	1	0	
1288		1	98	0	1	0	0	
1289		1	98	0	1	0	0	
1290		1	98	0	1	0	0	
1291		1	98	0	1	0	0	
1292		1	98	0	1	1	0	
1293		11	98	1	1	1	0	*Read CSR*
1294	FF		4C	0	1	1	0	
1295		1	98	0	1	1	0	
1296		1	98	0	1	1	0	
1297		1	98	0	1	0	0	
1298		1	98	0	1	0	0	
1299		1	98	0	1	0	0	
1300		1	98	0	1	0	0	

1301	1	98	0	1	1	0	
1302	11	98	1	1	1	0	***Read CSR***
1303 FF		42	0	1	1	0	
1304	1	98	0	1	1	0	
1305	1	98	0	1	1	0	
1306	1	98	0	1	0	0	
1307	8	98	0	1	0	0	
1308	8	98	0	1	0	0	
1309	8	98	0	1	0	0	
1310	8	98	0	1	1	0	
1311	16	98	1	1	1	0	***Read COU***
1312 FF		42	0	1	1	0	
1313	8	98	0	1	1	0	
1314	8	98	0	1	1	0	
1315	8	98	0	1	0	0	
1316	8	98	0	1	0	0	
1317	80	98	0	1	0	0	
1318	80	98	0	1	0	0	
1319	80	98	0	1	1	0	
1320	20	98	1	1	1	0	***Read Fifo,***
1321 FF		42	0	1	1	0	
1322	80	98	0	1	1	0	
1323	80	98	0	1	1	0	
1324	80	98	0	1	0	0	
1325	80	98	0	1	0	0	
1326	6	98	0	1	0	0	
1327	6	98	0	1	0	0	
1328	6	98	0	1	1	0	
1329	20	98	1	1	1	0	***Read Fifo,***
1330 FF		42	0	1	1	0	
1331	6	98	0	1	1	0	
1332	6	98	0	1	1	0	
1333	6	98	0	1	0	0	
1334	6	98	0	1	0	0	
1335	0	98	0	1	0	0	
1336	0	98	0	1	0	0	
1337	0	98	0	1	1	0	
1338	20	98	1	1	1	0	***Read Fifo,***
1339 FF		42	0	1	1	0	
1340	0	98	0	1	1	0	
1341	0	98	0	1	1	0	
1342	0	98	0	1	0	0	
1343	0	98	0	1	0	0	
1344	1	98	0	1	0	0	
1345	1	98	0	1	0	0	
1346	1	98	0	1	1	0	
1347	20	98	1	1	1	0	***Read Fifo,***
1348 FF		42	0	1	1	0	
1349	1	98	0	1	1	0	
1350	1	98	0	1	1	0	
1351	1	98	0	1	0	0	
1352	1	98	0	1	0	0	

1353	0	98	0	1	0	0	
1354	0	98	0	1	0	0	
1355	0	98	0	1	1	0	
1356	20	98	1	1	1	0	***Read Fifo,***
1357 FF		42	0	1	1	0	
1358	0	98	0	1	1	0	
1359	0	98	0	1	1	0	
1360	0	98	0	1	0	0	
1361	0	98	0	1	0	0	
1362	0	98	0	1	0	0	
1363	0	98	0	1	0	0	
1364	0	98	0	1	1	0	
1365	20	98	1	1	1	0	***Read Fifo,***
1366 FF		42	0	1	1	0	
1367	0	98	0	1	1	0	
1368	0	98	0	1	1	0	
1369	0	98	0	1	0	0	
1370	0	98	0	1	0	0	
1371	12	98	0	1	0	0	
1372	12	98	0	1	0	0	
1373	12	98	0	1	1	0	
1374	20	98	1	1	1	0	***Read Fifo,***
1375 FF		42	0	1	1	0	
1376	12	98	0	1	1	0	
1377	12	98	0	1	1	0	
1378	12	98	0	1	0	0	
1379	12	98	0	1	0	0	
1380	0	98	0	1	0	0	
1381	0	98	0	1	0	0	
1382	0	98	0	1	1	0	
1383	20	98	1	1	1	0	***Read Fifo,***
1384 FF		42	0	1	1	0	
1385	0	98	0	1	1	0	
1386	0	98	0	1	1	0	
1387	40	98	0	0	1	0	
1388	40	98	0	0	1	0	
1389	40	98	0	0	1	0	
1390	40	98	0	0	1	0	
1391	0	98	0	1	1	0	
1392	11	98	1	1	1	0	***Write CSR***
1393 FF		42	0	1	1	0	
1394	0	98	0	1	1	0	
1395	0	98	0	1	1	0	
1396	12	98	0	0	1	0	
1397	12	98	0	0	1	0	
1398	12	98	0	0	1	0	
1399	12	98	0	0	1	0	
1400	0	98	0	1	1	0	
1401	20	98	1	1	1	0	***Write Fifo,***
1402 FF		48	0	1	1	0	
1403	0	98	0	1	1	0	
1404	0	98	0	1	1	0	

1405	1	98	0	0	1	0	
1406	1	98	0	0	1	0	
1407	1	98	0	0	1	0	
1408	1	98	0	0	1	0	
1409	0	98	0	1	1	0	
1410	20	98	1	1	1	0	***Write Fifo,***
1411 FF		48	0	1	1	0	
1412	0	98	0	1	1	0	
1413	0	98	0	1	1	0	
1414	10	98	0	0	1	0	
1415	10	98	0	0	1	0	
1416	10	98	0	0	1	0	
1417	10	98	0	0	1	0	
1418	0	98	0	1	1	0	
1419	20	98	1	1	1	0	***Write Fifo,***
1420 FF		48	0	1	1	0	
1421	0	98	0	1	1	0	
1422	0	98	0	1	1	0	
1423	1	98	0	0	1	0	
1424	1	98	0	0	1	0	
1425	1	98	0	0	1	0	
1426	1	98	0	0	1	0	
1427	0	98	0	1	1	0	
1428	20	98	1	1	1	0	***Write Fifo,***
1429 FF		48	0	1	1	0	
1430	0	98	0	1	1	0	
1431	0	98	0	1	1	0	
1432	0	98	0	0	1	0	
1433	0	98	0	0	1	0	
1434	0	98	0	0	1	0	
1435	0	98	0	0	1	0	
1436	0	98	0	1	1	0	
1437	20	98	1	1	1	0	***Write Fifo,***
1438 FF		48	0	1	1	0	
1439	0	98	0	1	1	0	
1440	0	98	0	1	1	0	
1441	0	98	0	0	1	0	
1442	0	98	0	0	1	0	
1443	0	98	0	0	1	0	
1444	0	98	0	0	1	0	
1445	0	98	0	1	1	0	
1446	20	98	1	1	1	0	***Write Fifo,***
1447 FF		48	0	1	1	0	
1448	0	98	0	1	1	0	
1449	0	98	0	1	1	0	
1450	0	98	0	0	1	0	
1451	0	98	0	0	1	0	
1452	0	98	0	0	1	0	
1453	0	98	0	0	1	0	
1454	0	98	0	1	1	0	
1455	20	98	1	1	1	0	***Write Fifo,***
1456 FF		48	0	1	1	0	

1457	0	98	0	1	1	0	
1458	0	98	0	1	1	0	
1459	8	98	0	0	1	0	
1460	8	98	0	0	1	0	
1461	8	98	0	0	1	0	
1462	8	98	0	0	1	0	
1463	0	98	0	1	1	0	
1464	20	98	1	1	1	0	***Write Fifo,***
1465 FF		48	0	1	1	0	
1466	0	98	0	1	1	0	
1467	0	98	0	1	1	0	
1468	2	98	0	0	1	0	
1469	2	98	0	0	1	0	
1470	2	98	0	0	1	0	
1471	2	98	0	0	1	0	
1472	0	98	0	1	1	0	
1473	11	98	1	1	1	0	***Write C***
1474 FF		48	0	1	1	0	
1475 AA		21	0	1	1	1	***7th USB in***
1476 AA		21	0	1	1	1	
1477	8	21	1	1	1	1	
1478 AA		21	0	1	1	1	
1479	0	98	0	1	1	0	
1480	0	98	0	1	1	0	
1481	0	98	0	1	0	0	
1482	0	98	0	1	0	0	
1483	0	98	0	1	0	0	
1484	0	98	0	1	0	0	
1485	0	98	0	1	1	0	
1486	6	98	1	1	1	0	
1487 FF		50	0	1	1	0	
1488	0	98	0	1	1	0	
1489	0	98	0	1	1	0	
1490	0	98	0	1	0	0	
1491	1	98	0	1	0	0	
1492	1	98	0	1	0	0	
1493	1	98	0	1	0	0	
1494	1	98	0	1	1	0	
1495	2	98	1	1	1	0	***Read INTR***
1496 FF		50	0	1	1	0	
1497	1	98	0	1	1	0	
1498	1	98	0	1	1	0	
1499	1	98	0	1	0	0	
1500	0	98	0	1	0	0	
1501	0	98	0	1	0	0	
1502	0	98	0	1	0	0	
1503	0	98	0	1	1	0	
1504	3	98	1	1	1	0	
1505 FF		50	0	1	1	0	
1506	0	98	0	1	1	0	
1507	0	98	0	1	1	0	

1508	0	98	0	1	0	0	
1509	0	98	0	1	0	0	
1510	0	98	0	1	0	0	
1511	0	98	0	1	0	0	
1512	0	98	0	1	1	0	
1513	4	98	1	1	1	0	
1514 FF		50	0	1	1	0	
1515	0	98	0	1	1	0	
1516	0	98	0	1	1	0	
1517	0	98	0	1	0	0	
1518	0	98	0	1	0	0	
1519	0	98	0	1	0	0	
1520	0	98	0	1	0	0	
1521	0	98	0	1	1	0	
1522	5	98	1	1	1	0	
1523 FF		50	0	1	1	0	
1524	0	98	0	1	1	0	
1525	0	98	0	1	1	0	
1526	0	98	0	1	0	0	
1527	0	98	0	1	0	0	
1528	0	98	0	1	0	0	
1529	0	98	0	1	0	0	
1530	0	98	0	1	1	0	
1531	11	98	1	1	1	0	***Read CSR***
1532 FF	4B		0	1	1	0	
1533	0	98	0	1	1	0	
1534	0	98	0	1	1	0	
1535	0	98	0	1	0	0	
1536	1	98	0	1	0	0	
1537	1	98	0	1	0	0	
1538	1	98	0	1	0	0	
1539	1	98	0	1	1	0	
1540	1	98	1	1	1	0	***Read Pow***
1541 FF	4B		0	1	1	0	
1542	1	98	0	1	1	0	
1543	1	98	0	1	1	0	
1544	1	98	0	1	0	0	
1545	0	98	0	1	0	0	
1546	0	98	0	1	0	0	
1547	0	98	0	1	0	0	
1548	0	98	0	1	1	0	
1549 0E		98	1	1	1	0	***Read Inde***
1550 FF	4B		0	1	1	0	
1551	0	98	0	1	1	0	
1552	0	98	0	1	1	0	
1553	0	98	0	0	1	0	
1554	0	98	0	0	1	0	
1555	0	98	0	0	1	0	
1556	0	98	0	0	1	0	
1557	0	98	0	1	1	0	
1558 0E		98	1	1	1	0	***Write Inde***
1559 FF	4B		0	1	1	0	

1560	0	98	0	1	1	0	
1561	0	98	0	1	1	0	
1562	0	98	0	1	0	0	
1563	0	98	0	1	0	0	
1564	0	98	0	1	0	0	
1565	0	98	0	1	0	0	
1566	0	98	0	1	1	0	
1567	11	98	1	1	1	0	***Read CSR***
1568 FF	4C		0	1	1	0	
1569	0	98	0	1	1	0	
1570	0	98	0	1	1	0	
1571	0	98	0	1	0	0	
1572	0	98	0	1	0	0	
1573	0	98	0	1	0	0	
1574	0	98	0	1	0	0	
1575	0	98	0	1	1	0	
1576	11	98	1	1	1	0	***Read CSR***
1577 FF	4C		0	1	1	0	
1578	0	98	0	1	1	0	
1579	0	98	0	1	1	0	
1580 E0		98	0	0	1	0	
1581 E0		98	0	0	1	0	
1582 E0		98	0	0	1	0	
1583 E0		98	0	0	1	0	
1584	0	98	0	1	1	0	
1585	20	98	1	1	1	0	***Write fifo,***
1586 FF		48	0	1	1	0	
1587	0	98	0	1	1	0	
1588	0	98	0	1	1	0	
1589	5	98	0	0	1	0	
1590	5	98	0	0	1	0	
1591	5	98	0	0	1	0	
1592	5	98	0	0	1	0	
1593	0	98	0	1	1	0	
1594	20	98	1	1	1	0	***Write fifo,***
1595 FF		48	0	1	1	0	
1596	0	98	0	1	1	0	
1597	0	98	0	1	1	0	
1598	0	98	0	0	1	0	
1599	0	98	0	0	1	0	
1600	0	98	0	0	1	0	
1601	0	98	0	0	1	0	
1602	0	98	0	1	1	0	
1603	20	98	1	1	1	0	***Write fifo,***
1604 FF		48	0	1	1	0	
1605	0	98	0	1	1	0	
1606	0	98	0	1	1	0	
1607	2	98	0	0	1	0	
1608	2	98	0	0	1	0	
1609	2	98	0	0	1	0	
1610	2	98	0	0	1	0	
1611	0	98	0	1	1	0	

1612	20	98	**1**	1	1	0	***Write fifo,***
1613 FF		48	0	1	1	0	
1614	0	98	0	1	1	0	
1615	0	98	0	1	1	0	
1616	0	98	0	0	1	0	
1617	0	98	0	0	1	0	
1618	0	98	0	0	1	0	
1619	0	98	0	0	1	0	
1620	0	98	0	1	1	0	
1621	20	98	**1**	1	1	0	***Write fifo,***
1622 FF		48	0	1	1	0	
1623	0	98	0	1	1	0	
1624	0	98	0	1	1	0	
1625	3	98	0	0	1	0	
1626	3	98	0	0	1	0	
1627	3	98	0	0	1	0	
1628	3	98	0	0	1	0	
1629	0	98	0	1	1	0	
1630	20	98	**1**	1	1	0	***Write fifo,***
1631 FF		48	0	1	1	0	
1632	0	98	0	1	1	0	
1633	0	98	0	1	1	0	
1634	1	98	0	0	1	0	
1635	1	98	0	0	1	0	
1636	1	98	0	0	1	0	
1637	1	98	0	0	1	0	
1638	0	98	0	1	1	0	
1639	20	98	**1**	1	1	0	***Write fifo,***
1640 FF		48	0	1	1	0	
1641	0	98	0	1	1	0	
1642	0	98	0	1	1	0	
1643	2	98	0	0	1	0	
1644	2	98	0	0	1	0	
1645	2	98	0	0	1	0	
1646	2	98	0	0	1	0	
1647	0	98	0	1	1	0	
1648	20	98	**1**	1	1	0	***Write fifo,***
1649 FF		48	0	1	1	0	
1650	0	98	0	1	1	0	
1651	0	98	0	1	1	0	
1652	2	98	0	0	1	0	
1653	2	98	0	0	1	0	
1654	2	98	0	0	1	0	
1655	2	98	0	0	1	0	
1656	0	98	0	1	1	0	
1657	11	98	**1**	1	1	0	***Write CSR***
1658 FF		48	0	1	1	0	
1659	83	50	0	1	1	**1**	***8th USB in***
1660	83	50	0	1	1	**1**	
1661 B8		50	**1**	1	1	**1**	
1662	83	50	0	1	1	**1**	
1663	0	98	0	1	1	0	

1664	0	98	0	1	1	0	
1665	0	98	0	1	0	0	
1666	0	98	0	1	0	0	
1667	0	98	0	1	0	0	
1668	0	98	0	1	0	0	
1669	0	98	0	1	1	0	
1670	6	98	1	1	1	0	
1671 FF		50	0	1	1	0	
1672	0	98	0	1	1	0	
1673	0	98	0	1	1	0	
1674	0	98	0	1	0	0	
1675	1	98	0	1	0	0	
1676	1	98	0	1	0	0	
1677	1	98	0	1	0	0	
1678	1	98	0	1	1	0	
1679	2	98	1	1	1	0	***Read INTR***
1680 FF		50	0	1	1	0	
1681	1	98	0	1	1	0	
1682	1	98	0	1	1	0	
1683	1	98	0	1	0	0	
1684	0	98	0	1	0	0	
1685	0	98	0	1	0	0	
1686	0	98	0	1	0	0	
1687	0	98	0	1	1	0	
1688	3	98	1	1	1	0	
1689 FF		50	0	1	1	0	
1690	0	98	0	1	1	0	
1691	0	98	0	1	1	0	
1692	0	98	0	1	0	0	
1693	0	98	0	1	0	0	
1694	0	98	0	1	0	0	
1695	0	98	0	1	0	0	
1696	0	98	0	1	1	0	
1697	4	98	1	1	1	0	
1698 FF		50	0	1	1	0	
1699	0	98	0	1	1	0	
1700	0	98	0	1	1	0	
1701	0	98	0	1	0	0	
1702	0	98	0	1	0	0	
1703	0	98	0	1	0	0	
1704	0	98	0	1	0	0	
1705	0	98	0	1	1	0	
1706	5	98	1	1	1	0	
1707 FF		50	0	1	1	0	
1708	0	98	0	1	1	0	
1709	0	98	0	1	1	0	
1710	0	98	0	1	0	0	
1711	0	98	0	1	0	0	
1712	0	98	0	1	0	0	
1713	0	98	0	1	0	0	
1714	0	98	0	1	1	0	
1715	11	98	1	1	1	0	***Read CSR***

1716 FF	4B		0	1	1	0	
1717	0	98	0	1	1	0	
1718	0	98	0	1	1	0	
1719	0	98	0	1	0	0	
1720	1	98	0	1	0	0	
1721	1	98	0	1	0	0	
1722	1	98	0	1	0	0	
1723	1	98	0	1	1	0	
1724	1	98	1	1	1	0	***Read Pow***
1725 FF	4B		0	1	1	0	
1726	1	98	0	1	1	0	
1727	1	98	0	1	1	0	
1728	1	98	0	1	0	0	
1729	0	98	0	1	0	0	
1730	0	98	0	1	0	0	
1731	0	98	0	1	0	0	
1732	0	98	0	1	1	0	
1733 0E		98	1	1	1	0	***Read Inde***
1734 FF	4B		0	1	1	0	
1735	0	98	0	1	1	0	
1736	0	98	0	1	1	0	
1737	0	98	0	0	1	0	
1738	0	98	0	0	1	0	
1739	0	98	0	0	1	0	
1740	0	98	0	0	1	0	
1741	0	98	0	1	1	0	
1742 0E		98	1	1	1	0	***Write Inde***
1743 FF	4B		0	1	1	0	
1744	0	98	0	1	1	0	
1745	0	98	0	1	1	0	
1746	0	98	0	1	0	0	
1747	0	98	0	1	0	0	
1748	0	98	0	1	0	0	
1749	0	98	0	1	0	0	
1750	0	98	0	1	1	0	
1751	11	98	1	1	1	0	***Read CSR***
1752 FF	4C		0	1	1	0	
1753	0	98	0	1	1	0	
1754	0	98	0	1	1	0	
1755	0	98	0	1	0	0	
1756	0	98	0	1	0	0	
1757	0	98	0	1	0	0	
1758	0	98	0	1	0	0	
1759	0	98	0	1	1	0	
1760	11	98	1	1	1	0	***Read CSR***
1761 FF	4C		0	1	1	0	
1762	0	98	0	1	1	0	
1763	0	98	0	1	1	0	
1764	3	98	0	0	1	0	
1765	3	98	0	0	1	0	
1766	3	98	0	0	1	0	
1767	3	98	0	0	1	0	

1768		0	98	0	1	1	0	
1769		20	98	1	1	1	0	***Write Fifo***
1770	FF		48	0	1	1	0	
1771		0	98	0	1	1	0	
1772		0	98	0	1	1	0	
1773		1	98	0	0	1	0	
1774		1	98	0	0	1	0	
1775		1	98	0	0	1	0	
1776		1	98	0	0	1	0	
1777		0	98	0	1	1	0	
1778		20	98	1	1	1	0	***Write Fifo***
1779	FF		48	0	1	1	0	
1780		0	98	0	1	1	0	
1781		0	98	0	1	1	0	
1782	0A		98	0	0	1	0	
1783	0A		98	0	0	1	0	
1784	0A		98	0	0	1	0	
1785	0A		98	0	0	1	0	
1786		0	98	0	1	1	0	
1787		11	98	1	1	1	0	***Write CSR***
1788	FF		48	0	1	1	0	
1789	B4	4C		0	1	1	1	***9th USB in***
1790	B4	4C		0	1	1	1	
1791		57 4C		1	1	1	1	
1792	B4	4C		0	1	1	1	
1793		0	98	0	1	1	0	
1794		0	98	0	1	1	0	
1795		0	98	0	1	0	0	
1796		0	98	0	1	0	0	
1797		0	98	0	1	0	0	
1798		0	98	0	1	0	0	
1799		0	98	0	1	1	0	
1800		6	98	1	1	1	0	
1801	FF		50	0	1	1	0	
1802		0	98	0	1	1	0	
1803		0	98	0	1	1	0	
1804		0	98	0	1	0	0	
1805		1	98	0	1	0	0	
1806		1	98	0	1	0	0	
1807		1	98	0	1	0	0	
1808		1	98	0	1	1	0	
1809		2	98	1	1	1	0	***Read INTR***
1810	FF		50	0	1	1	0	
1811		1	98	0	1	1	0	
1812		1	98	0	1	1	0	
1813		1	98	0	1	0	0	
1814		0	98	0	1	0	0	
1815		0	98	0	1	0	0	
1816		0	98	0	1	0	0	
1817		0	98	0	1	1	0	
1818		3	98	1	1	1	0	
1819	FF		50	0	1	1	0	

1820	0	98	0	1	1	0	
1821	0	98	0	1	1	0	
1822	0	98	0	1	0	0	
1823	0	98	0	1	0	0	
1824	0	98	0	1	0	0	
1825	0	98	0	1	0	0	
1826	0	98	0	1	1	0	
1827	4	98	1	1	1	0	
1828 FF		50	0	1	1	0	
1829	0	98	0	1	1	0	
1830	0	98	0	1	1	0	
1831	0	98	0	1	0	0	
1832	0	98	0	1	0	0	
1833	0	98	0	1	0	0	
1834	0	98	0	1	0	0	
1835	0	98	0	1	1	0	
1836	5	98	1	1	1	0	
1837 FF		50	0	1	1	0	
1838	0	98	0	1	1	0	
1839	0	98	0	1	1	0	
1840	0	98	0	1	0	0	
1841	0	98	0	1	0	0	
1842	0	98	0	1	0	0	
1843	0	98	0	1	0	0	
1844	0	98	0	1	1	0	
1845	11	98	1	1	1	0	***Read CSR***
1846 FF	4B		0	1	1	0	
1847	0	98	0	1	1	0	
1848	0	98	0	1	1	0	
1849	0	98	0	1	0	0	
1850	1	98	0	1	0	0	
1851	1	98	0	1	0	0	
1852	1	98	0	1	0	0	
1853	1	98	0	1	1	0	
1854	1	98	1	1	1	0	***Read Pow***
1855 FF	4B		0	1	1	0	
1856	1	98	0	1	1	0	
1857	1	98	0	1	1	0	
1858	1	98	0	1	0	0	
1859	0	98	0	1	0	0	
1860	0	98	0	1	0	0	
1861	0	98	0	1	0	0	
1862	0	98	0	1	1	0	
1863 0E		98	1	1	1	0	***Read Inde***
1864 FF	4B		0	1	1	0	
1865	0	98	0	1	1	0	
1866	0	98	0	1	1	0	
1867	0	98	0	0	1	0	
1868	0	98	0	0	1	0	
1869	0	98	0	0	1	0	
1870	0	98	0	0	1	0	
1871	0	98	0	1	1	0	

1872	0E		98	1	1	1	0	*Write inde*
1873	FF	4B		0	1	1	0	
1874		0	98	0	1	1	0	
1875		0	98	0	1	1	0	
1876		0	98	0	1	0	0	
1877		0	98	0	1	0	0	
1878		0	98	0	1	0	0	
1879		0	98	0	1	0	0	
1880		0	98	0	1	1	0	
1881		11	98	1	1	1	0	*Read CSR*
1882	FF	4C		0	1	1	0	
1883		0	98	0	1	1	0	
1884		0	98	0	1	1	0	
1885		0	98	0	1	0	0	
1886		0	98	0	1	0	0	
1887		0	98	0	1	0	0	
1888		0	98	0	1	0	0	
1889		0	98	0	1	1	0	
1890		11	98	1	1	1	0	*Read CSR*
1891	FF	4C		0	1	1	0	
1892		0	98	0	1	1	0	
1893		0	98	0	1	1	0	
1894		0	98	0	1	0	0	
1895		0	98	0	1	0	0	
1896		0	98	0	1	0	0	
1897		0	98	0	1	0	0	
1898		0	98	0	1	1	0	
1899		11	98	1	1	1	0	*Read CSR*
1900	FF		42	0	1	1	0	
1901	F5		42	0	1	1	1	*10th USB i*
1902	F5		42	0	1	1	1	
1903		39	42	1	1	1	1	
1904	F5		42	0	1	1	1	
1905		0	98	0	1	1	0	
1906		0	98	0	1	1	0	
1907		0	98	0	1	0	0	
1908		0	98	0	1	0	0	
1909		0	98	0	1	0	0	
1910		0	98	0	1	0	0	
1911		0	98	0	1	1	0	
1912		6	98	1	1	1	0	
1913	FF		50	0	1	1	0	
1914		0	98	0	1	1	0	
1915		0	98	0	1	1	0	
1916		0	98	0	1	0	0	
1917		1	98	0	1	0	0	
1918		1	98	0	1	0	0	
1919		1	98	0	1	0	0	
1920		1	98	0	1	1	0	
1921		2	98	1	1	1	0	*Read INTR*
1922	FF		50	0	1	1	0	
1923		1	98	0	1	1	0	

1924	1	98	0	1	1	0	
1925	1	98	0	1	0	0	
1926	0	98	0	1	0	0	
1927	0	98	0	1	0	0	
1928	0	98	0	1	0	0	
1929	0	98	0	1	1	0	
1930	3	98	1	1	1	0	
1931 FF		50	0	1	1	0	
1932	0	98	0	1	1	0	
1933	0	98	0	1	1	0	
1934	0	98	0	1	0	0	
1935	0	98	0	1	0	0	
1936	0	98	0	1	0	0	
1937	0	98	0	1	0	0	
1938	0	98	0	1	1	0	
1939	4	98	1	1	1	0	
1940 FF		50	0	1	1	0	
1941	0	98	0	1	1	0	
1942	0	98	0	1	1	0	
1943	0	98	0	1	0	0	
1944	0	98	0	1	0	0	
1945	0	98	0	1	0	0	
1946	0	98	0	1	0	0	
1947	0	98	0	1	1	0	
1948	5	98	1	1	1	0	
1949 FF		50	0	1	1	0	
1950	0	98	0	1	1	0	
1951	0	98	0	1	1	0	
1952	0	98	0	1	0	0	
1953	1	98	0	1	0	0	
1954	1	98	0	1	0	0	
1955	1	98	0	1	0	0	
1956	1	98	0	1	1	0	
1957	11	98	1	1	1	0	***Read CSR***
1958 FF	4B		0	1	1	0	
1959	1	98	0	1	1	0	
1960	1	98	0	1	1	0	
1961	1	98	0	1	0	0	
1962	0	98	0	1	0	0	
1963	0	98	0	1	0	0	
1964	0	98	0	1	0	0	
1965	0	98	0	1	1	0	
1966 0E		98	1	1	1	0	***Read Inde***
1967 FF	4B		0	1	1	0	
1968	0	98	0	1	1	0	
1969	0	98	0	1	1	0	
1970	0	98	0	0	1	0	
1971	0	98	0	0	1	0	
1972	0	98	0	0	1	0	
1973	0	98	0	0	1	0	
1974	0	98	0	1	1	0	
1975 0E		98	1	1	1	0	***Write Inde***

1976 FF	4B		0	1	1	0	
1977	0	98	0	1	1	0	
1978	0	98	0	1	1	0	
1979	0	98	0	1	0	0	
1980	1	98	0	1	0	0	
1981	1	98	0	1	0	0	
1982	1	98	0	1	0	0	
1983	1	98	0	1	1	0	
1984	11	98	1	1	1	0	***Read CSR***
1985 FF	4C		0	1	1	0	
1986	1	98	0	1	1	0	
1987	1	98	0	1	1	0	
1988	1	98	0	1	0	0	
1989	1	98	0	1	0	0	
1990	1	98	0	1	0	0	
1991	1	98	0	1	0	0	
1992	1	98	0	1	1	0	
1993	11	98	1	1	1	0	***Read CSR***
1994 FF	4C		0	1	1	0	
1995	1	98	0	1	1	0	
1996	1	98	0	1	1	0	
1997	1	98	0	1	0	0	
1998	1	98	0	1	0	0	
1999	1	98	0	1	0	0	
2000	1	98	0	1	0	0	
2001	1	98	0	1	1	0	
2002	11	98	1	1	1	0	***Read CSR***
2003 FF		42	0	1	1	0	
2004	1	98	0	1	1	0	
2005	1	98	0	1	1	0	
2006	1	98	0	1	0	0	
2007	8	98	0	1	0	0	
2008	8	98	0	1	0	0	
2009	8	98	0	1	0	0	
2010	8	98	0	1	1	0	
2011	16	98	1	1	1	0	***Read OUT***
2012 FF		42	0	1	1	0	
2013	8	98	0	1	1	0	
2014	8	98	0	1	1	0	
2015	8	98	0	1	0	0	
2016	8	98	0	1	0	0	
2017	80	98	0	1	0	0	
2018	80	98	0	1	0	0	
2019	80	98	0	1	1	0	
2020	20	98	1	1	1	0	***Read Fifo,***
2021 FF		42	0	1	1	0	
2022	80	98	0	1	1	0	
2023	80	98	0	1	1	0	
2024	80	98	0	1	0	0	
2025	80	98	0	1	0	0	
2026	6	98	0	1	0	0	
2027	6	98	0	1	0	0	

2028	6	98	0	1	1	0	
2029	20	98	**1**	1	1	0	***Read Fifo,***
2030 FF		42	0	1	1	0	
2031	6	98	0	1	1	0	
2032	6	98	0	1	1	0	
2033	6	98	0	1	0	0	
2034	6	98	0	1	0	0	
2035	0	98	0	1	0	0	
2036	0	98	0	1	0	0	
2037	0	98	0	1	1	0	
2038	20	98	**1**	1	1	0	***Read Fifo,***
2039 FF		42	0	1	1	0	
2040	0	98	0	1	1	0	
2041	0	98	0	1	1	0	
2042	0	98	0	1	0	0	
2043	0	98	0	1	0	0	
2044	2	98	0	1	0	0	
2045	2	98	0	1	0	0	
2046	2	98	0	1	1	0	
2047	20	98	**1**	1	1	0	***Read Fifo,***
2048 FF		42	0	1	1	0	
2049	2	98	0	1	1	0	
2050	2	98	0	1	1	0	
2051	2	98	0	1	0	0	
2052	2	98	0	1	0	0	
2053	0	98	0	1	0	0	
2054	0	98	0	1	0	0	
2055	0	98	0	1	1	0	
2056	20	98	**1**	1	1	0	***Read fifo,***
2057 FF		42	0	1	1	0	
2058	0	98	0	1	1	0	
2059	0	98	0	1	1	0	
2060	0	98	0	1	0	0	
2061	0	98	0	1	0	0	
2062	0	98	0	1	0	0	
2063	0	98	0	1	0	0	
2064	0	98	0	1	1	0	
2065	20	98	**1**	1	1	0	***Read fifo,***
2066 FF		42	0	1	1	0	
2067	0	98	0	1	1	0	
2068	0	98	0	1	1	0	
2069	0	98	0	1	0	0	
2070	0	98	0	1	0	0	
2071	9	98	0	1	0	0	
2072	9	98	0	1	0	0	
2073	9	98	0	1	1	0	
2074	20	98	**1**	1	1	0	***Read fifo,***
2075 FF		42	0	1	1	0	
2076	9	98	0	1	1	0	
2077	9	98	0	1	1	0	
2078	9	98	0	1	0	0	
2079	9	98	0	1	0	0	

2080	0	98	0	1	0	0	
2081	0	98	0	1	0	0	
2082	0	98	0	1	1	0	
2083	20	98	1	1	1	0	***Read fifo,***
2084 FF		42	0	1	1	0	
2085	0	98	0	1	1	0	
2086	0	98	0	1	1	0	
2087	40	98	0	0	1	0	
2088	40	98	0	0	1	0	
2089	40	98	0	0	1	0	
2090	40	98	0	0	1	0	
2091	0	98	0	1	1	0	
2092	11	98	1	1	1	0	***Write CSR***
2093 FF		42	0	1	1	0	
2094	0	98	0	1	1	0	
2095	0	98	0	1	1	0	
2096	9	98	0	0	1	0	
2097	9	98	0	0	1	0	
2098	9	98	0	0	1	0	
2099	9	98	0	0	1	0	
2100	0	98	0	1	1	0	
2101	20	98	1	1	1	0	***Write fifo***
2102 FF		48	0	1	1	0	
2103	0	98	0	1	1	0	
2104	0	98	0	1	1	0	
2105	2	98	0	0	1	0	
2106	2	98	0	0	1	0	
2107	2	98	0	0	1	0	
2108	2	98	0	0	1	0	
2109	0	98	0	1	1	0	
2110	20	98	1	1	1	0	***Write fifo***
2111 FF		48	0	1	1	0	
2112	0	98	0	1	1	0	
2113	0	98	0	1	1	0	
2114	22	98	0	0	1	0	
2115	22	98	0	0	1	0	
2116	22	98	0	0	1	0	
2117	22	98	0	0	1	0	
2118	0	98	0	1	1	0	
2119	20	98	1	1	1	0	***Write fifo***
2120 FF		48	0	1	1	0	
2121	0	98	0	1	1	0	
2122	0	98	0	1	1	0	
2123	0	98	0	0	1	0	
2124	0	98	0	0	1	0	
2125	0	98	0	0	1	0	
2126	0	98	0	0	1	0	
2127	0	98	0	1	1	0	
2128	20	98	1	1	1	0	***Write fifo***
2129 FF		48	0	1	1	0	
2130	0	98	0	1	1	0	
2131	0	98	0	1	1	0	

2132	1	98	0	0	1	0	
2133	1	98	0	0	1	0	
2134	1	98	0	0	1	0	
2135	1	98	0	0	1	0	
2136	0	98	0	1	1	0	
2137	20	98	1	1	1	0	***Write fifo***
2138 FF		48	0	1	1	0	
2139	0	98	0	1	1	0	
2140	0	98	0	1	1	0	
2141	1	98	0	0	1	0	
2142	1	98	0	0	1	0	
2143	1	98	0	0	1	0	
2144	1	98	0	0	1	0	
2145	0	98	0	1	1	0	
2146	20	98	1	1	1	0	***Write fifo***
2147 FF		48	0	1	1	0	
2148	0	98	0	1	1	0	
2149	0	98	0	1	1	0	
2150	4	98	0	0	1	0	
2151	4	98	0	0	1	0	
2152	4	98	0	0	1	0	
2153	4	98	0	0	1	0	
2154	0	98	0	1	1	0	
2155	20	98	1	1	1	0	***Write fifo***
2156 FF		48	0	1	1	0	
2157	0	98	0	1	1	0	
2158	0	98	0	1	1	0	
2159 C0		98	0	0	1	0	
2160 C0		98	0	0	1	0	
2161 C0		98	0	0	1	0	
2162 C0		98	0	0	1	0	
2163	0	98	0	1	1	0	
2164	20	98	1	1	1	0	***Write fifo***
2165 FF		48	0	1	1	0	
2166	0	98	0	1	1	0	
2167	0	98	0	1	1	0	
2168	2	98	0	0	1	0	
2169	2	98	0	0	1	0	
2170	2	98	0	0	1	0	
2171	2	98	0	0	1	0	
2172	0	98	0	1	1	0	
2173	11	98	1	1	1	0	***Write CSR***
2174 FF		48	0	1	1	0	
2175	82	50	0	1	1	1	***11th USB i***
2176 D0		50	0	1	1	1	
2177 D0		50	0	1	1	1	
2178 B7		50	1	1	1	1	
2179	0	98	0	1	1	0	
2180	0	98	0	1	1	0	
2181	0	98	0	1	0	0	
2182	0	98	0	1	0	0	
2183	0	98	0	1	0	0	

2184	0	98	0	1	0	0
2185	0	98	0	1	1	0
2186	6	98	1	1	1	0
2187 FF		50	0	1	1	0
2188	0	98	0	1	1	0
2189	0	98	0	1	1	0
2190	0	98	0	1	0	0
2191	1	98	0	1	0	0
2192	1	98	0	1	0	0
2193	1	98	0	1	0	0
2194	1	98	0	1	1	0
2195	2	98	1	1	1	0
2196 FF		50	0	1	1	0
2197	1	98	0	1	1	0
2198	1	98	0	1	1	0
2199	1	98	0	1	0	0
2200	0	98	0	1	0	0
2201	0	98	0	1	0	0
2202	0	98	0	1	0	0
2203	0	98	0	1	1	0
2204	3	98	1	1	1	0
2205 FF		50	0	1	1	0
2206	0	98	0	1	1	0
2207	0	98	0	1	1	0
2208	0	98	0	1	0	0
2209	0	98	0	1	0	0
2210	0	98	0	1	0	0
2211	0	98	0	1	0	0
2212	0	98	0	1	1	0
2213	4	98	1	1	1	0
2214 FF		50	0	1	1	0
2215	0	98	0	1	1	0
2216	0	98	0	1	1	0
2217	0	98	0	1	0	0
2218	0	98	0	1	0	0
2219	0	98	0	1	0	0
2220	0	98	0	1	0	0
2221	0	98	0	1	1	0
2222	5	98	1	1	1	0
2223 FF		50	0	1	1	0
2224	0	98	0	1	1	0
2225	0	98	0	1	1	0
2226	0	98	0	1	0	0
2227	0	98	0	1	0	0
2228	0	98	0	1	0	0
2229	0	98	0	1	0	0
2230	0	98	0	1	1	0
2231	11	98	1	1	1	0
2232 FF	4B		0	1	1	0
2233	0	98	0	1	1	0
2234	0	98	0	1	1	0
2235	0	98	0	1	0	0

2236	1	98	0	1	0	0
2237	1	98	0	1	0	0
2238	1	98	0	1	0	0
2239	1	98	0	1	1	0
2240	1	98	1	1	1	0
2241 FF	4B		0	1	1	0
2242	1	98	0	1	1	0
2243	1	98	0	1	1	0
2244	1	98	0	1	0	0
2245	0	98	0	1	0	0
2246	0	98	0	1	0	0
2247	0	98	0	1	0	0
2248	0	98	0	1	1	0
2249 0E		98	1	1	1	0
2250 FF	4B		0	1	1	0
2251	0	98	0	1	1	0
2252	0	98	0	1	1	0
2253	0	98	0	0	1	0
2254	0	98	0	0	1	0
2255	0	98	0	0	1	0
2256	0	98	0	0	1	0
2257	0	98	0	1	1	0
2258 0E		98	1	1	1	0
2259 FF	4B		0	1	1	0
2260	0	98	0	1	1	0
2261	0	98	0	1	1	0
2262	0	98	0	1	0	0
2263	0	98	0	1	0	0
2264	0	98	0	1	0	0
2265	0	98	0	1	0	0
2266	0	98	0	1	1	0
2267	11	98	1	1	1	0
2268 FF	4C		0	1	1	0
2269	0	98	0	1	1	0
2270	0	98	0	1	1	0
2271	0	98	0	1	0	0
2272	0	98	0	1	0	0
2273	0	98	0	1	0	0
2274	0	98	0	1	0	0
2275	0	98	0	1	1	0
2276	11	98	1	1	1	0
2277 FF	4C		0	1	1	0
2278	0	98	0	1	1	0
2279	0	98	0	1	1	0
2280	32	98	0	0	1	0
2281	32	98	0	0	1	0
2282	32	98	0	0	1	0
2283	32	98	0	0	1	0
2284	0	98	0	1	1	0
2285	20	98	1	1	1	0
2286 FF		48	0	1	1	0
2287	0	98	0	1	1	0

2288	0	98	0	1	1	0
2289	0A	98	0	0	1	0
2290	0A	98	0	0	1	0
2291	0A	98	0	0	1	0
2292	0A	98	0	0	1	0
2293	0	98	0	1	1	0
2294	11	98	1	1	1	0
2295	FF	48	0	1	1	0
2296	2	50	0	1	1	1
2297	D0	50	0	1	1	1
2298	D0	50	0	1	1	1
2299	AF	50	1	1	1	1
2300	0	98	0	1	1	0
2301	0	98	0	1	1	0
2302	0	98	0	1	0	0
2303	0	98	0	1	0	0
2304	0	98	0	1	0	0
2305	0	98	0	1	0	0
2306	0	98	0	1	1	0
2307	6	98	1	1	1	0
2308	FF	50	0	1	1	0
2309	0	98	0	1	1	0
2310	0	98	0	1	1	0
2311	0	98	0	1	0	0
2312	1	98	0	1	0	0
2313	1	98	0	1	0	0
2314	1	98	0	1	0	0
2315	1	98	0	1	1	0
2316	2	98	1	1	1	0
2317	FF	50	0	1	1	0
2318	1	98	0	1	1	0
2319	1	98	0	1	1	0
2320	1	98	0	1	0	0
2321	0	98	0	1	0	0
2322	0	98	0	1	0	0
2323	0	98	0	1	0	0
2324	0	98	0	1	1	0
2325	3	98	1	1	1	0
2326	FF	50	0	1	1	0
2327	0	98	0	1	1	0
2328	0	98	0	1	1	0
2329	0	98	0	1	0	0
2330	0	98	0	1	0	0
2331	0	98	0	1	0	0
2332	0	98	0	1	0	0
2333	0	98	0	1	1	0
2334	4	98	1	1	1	0
2335	FF	50	0	1	1	0
2336	0	98	0	1	1	0
2337	0	98	0	1	1	0
2338	0	98	0	1	0	0
2339	0	98	0	1	0	0

2340	0	98	0	1	0	0
2341	0	98	0	1	0	0
2342	0	98	0	1	1	0
2343	5	98	1	1	1	0
2344 FF		50	0	1	1	0
2345 8F		50	0	1	1	1
2346	46	50	0	1	1	1
2347	46	50	0	1	1	1
2348 6A		50	1	1	1	1
2349	0	98	0	1	1	0
2350	0	98	0	1	1	0
2351	0	98	0	1	0	0
2352	0	98	0	1	0	0
2353	0	98	0	1	0	0
2354	0	98	0	1	0	0
2355	0	98	0	1	1	0
2356	11	98	1	1	1	0
2357 FF	4B		0	1	1	0
2358	0	98	0	1	1	0
2359	0	98	0	1	1	0
2360	0	98	0	1	0	0
2361	1	98	0	1	0	0
2362	1	98	0	1	0	0
2363	1	98	0	1	0	0
2364	1	98	0	1	1	0
2365	1	98	1	1	1	0
2366 FF	4B		0	1	1	0
2367	1	98	0	1	1	0
2368	1	98	0	1	1	0
2369	1	98	0	1	0	0
2370	0	98	0	1	0	0
2371	0	98	0	1	0	0
2372	0	98	0	1	0	0
2373	0	98	0	1	1	0
2374 0E		98	1	1	1	0
2375 FF	4B		0	1	1	0
2376	0	98	0	1	1	0
2377	0	98	0	1	1	0
2378	0	98	0	0	1	0
2379	0	98	0	0	1	0
2380	0	98	0	0	1	0
2381	0	98	0	0	1	0
2382	0	98	0	1	1	0
2383 0E		98	1	1	1	0
2384 FF	4B		0	1	1	0
2385	0	98	0	1	1	0
2386	0	98	0	1	1	0
2387	0	98	0	1	0	0
2388	0	98	0	1	0	0
2389	0	98	0	1	0	0
2390	0	98	0	1	0	0
2391	0	98	0	1	1	0

2392	11	98	1	1	1	0
2393 FF	4C		0	1	1	0
2394	0	98	0	1	1	0
2395	0	98	0	1	1	0
2396	0	98	0	1	0	0
2397	0	98	0	1	0	0
2398	0	98	0	1	0	0
2399	0	98	0	1	0	0
2400	0	98	0	1	1	0
2401	11	98	1	1	1	0
2402 FF	4C		0	1	1	0
2403	0	98	0	1	1	0
2404	0	98	0	1	1	0
2405	0	98	0	1	0	0
2406	0	98	0	1	0	0
2407	0	98	0	1	0	0
2408	0	98	0	1	0	0
2409	0	98	0	1	1	0
2410	11	98	1	1	1	0
2411 FF		42	0	1	1	0
2412	0	98	0	1	1	0
2413	0	98	0	1	1	0
2414	0	98	0	1	0	0
2415	0	98	0	1	0	0
2416	0	98	0	1	0	0
2417	0	98	0	1	0	0
2418	0	98	0	1	1	0
2419	6	98	1	1	1	0
2420 FF		50	0	1	1	0
2421	0	98	0	1	1	0
2422	0	98	0	1	1	0
2423	0	98	0	1	0	0
2424	1	98	0	1	0	0
2425	1	98	0	1	0	0
2426	1	98	0	1	0	0
2427	1	98	0	1	1	0
2428	2	98	1	1	1	0
2429 FF		50	0	1	1	0
2430	1	98	0	1	1	0
2431	1	98	0	1	1	0
2432	1	98	0	1	0	0
2433	0	98	0	1	0	0
2434	0	98	0	1	0	0
2435	0	98	0	1	0	0
2436	0	98	0	1	1	0
2437	3	98	1	1	1	0
2438 FF		50	0	1	1	0
2439	0	98	0	1	1	0
2440	0	98	0	1	1	0
2441	0	98	0	1	0	0
2442	0	98	0	1	0	0
2443	0	98	0	1	0	0

2444	0	98	0	1	0	0
2445	0	98	0	1	1	0
2446	4	98	1	1	1	0
2447 FF		50	0	1	1	0
2448	0	98	0	1	1	0
2449	0	98	0	1	1	0
2450	0	98	0	1	0	0
2451	0	98	0	1	0	0
2452	0	98	0	1	0	0
2453	0	98	0	1	0	0
2454	0	98	0	1	1	0
2455	5	98	1	1	1	0
2456 FF		50	0	1	1	0
2457	0	98	0	1	1	0
2458	0	98	0	1	1	0
2459	0	98	0	1	0	0
2460	0	98	0	1	0	0
2461	0	98	0	1	0	0
2462	0	98	0	1	0	0
2463	0	98	0	1	1	0
2464	11	98	1	1	1	0
2465 FF	4B		0	1	1	0
2466	0	98	0	1	1	0
2467	0	98	0	1	1	0
2468	0	98	0	1	0	0
2469	1	98	0	1	0	0
2470	1	98	0	1	0	0
2471	1	98	0	1	0	0
2472	1	98	0	1	1	0
2473	1	98	1	1	1	0
2474 FF	4B		0	1	1	0
2475	1	98	0	1	1	0
2476	1	98	0	1	1	0
2477	1	98	0	1	0	0
2478	0	98	0	1	0	0
2479	0	98	0	1	0	0
2480	0	98	0	1	0	0
2481	0	98	0	1	1	0
2482 0E		98	1	1	1	0
2483 FF	4B		0	1	1	0
2484	0	98	0	1	1	0
2485	0	98	0	1	1	0
2486	0	98	0	0	1	0
2487	0	98	0	0	1	0
2488	0	98	0	0	1	0
2489	0	98	0	0	1	0
2490	0	98	0	1	1	0
2491 0E		98	1	1	1	0
2492 FF	4B		0	1	1	0
2493	0	98	0	1	1	0
2494	0	98	0	1	1	0
2495	0	98	0	1	0	0

2496	0	98	0	1	0	0
2497	0	98	0	1	0	0
2498	0	98	0	1	0	0
2499	0	98	0	1	1	0
2500	11	98	1	1	1	0
2501 FF	4C		0	1	1	0
2502	0	98	0	1	1	0
2503	0	98	0	1	1	0
2504	0	98	0	1	0	0
2505	0	98	0	1	0	0
2506	0	98	0	1	0	0
2507	0	98	0	1	0	0
2508	0	98	0	1	1	0
2509	11	98	1	1	1	0
2510 FF	4C		0	1	1	0
2511	0	98	0	1	1	0
2512	0	98	0	1	1	0
2513	0	98	0	1	0	0
2514	0	98	0	1	0	0
2515	0	98	0	1	0	0
2516	0	98	0	1	0	0
2517	0	98	0	1	1	0
2518	11	98	1	1	1	0
2519 FF		42	0	1	1	0
2520	3	41	0	1	1	1
2521 A0		41	1	1	1	1
2522	3	41	0	1	1	1
2523 FF	4F		0	1	1	1
2524	2	41	0	1	1	1
2525	2	41	0	1	1	0
2526	0	98	0	1	1	0
2527	0	98	0	1	1	0
2528	0	98	0	1	0	0
2529	0	98	0	1	0	0
2530	0	98	0	1	0	0
2531	0	98	0	1	0	0
2532	0	98	0	1	1	0
2533	6	98	1	1	1	0
2534 FF		50	0	1	1	0
2535	0	98	0	1	1	0
2536	0	98	0	1	1	0
2537	0	98	0	1	0	0
2538	1	98	0	1	0	0
2539	1	98	0	1	0	0
2540	1	98	0	1	0	0
2541	1	98	0	1	1	0
2542	2	98	1	1	1	0
2543 FF		50	0	1	1	0
2544	1	98	0	1	1	0
2545	1	98	0	1	1	0
2546	1	98	0	1	0	0
2547	0	98	0	1	0	0

2548	0	98	0	1	0	0
2549	0	98	0	1	0	0
2550	0	98	0	1	1	0
2551	3	98	1	1	1	0
2552 FF		50	0	1	1	0
2553	0	98	0	1	1	0
2554	0	98	0	1	1	0
2555	0	98	0	1	0	0
2556	0	98	0	1	0	0
2557	0	98	0	1	0	0
2558	0	98	0	1	0	0
2559	0	98	0	1	1	0
2560	4	98	1	1	1	0
2561 FF		50	0	1	1	0
2562	0	98	0	1	1	0
2563	0	98	0	1	1	0
2564	0	98	0	1	0	0
2565	0	98	0	1	0	0
2566	0	98	0	1	0	0
2567	0	98	0	1	0	0
2568	0	98	0	1	1	0
2569	5	98	1	1	1	0
2570 FF		50	0	1	1	0
2571	0	98	0	1	1	0
2572	0	98	0	1	1	0
2573	0	98	0	1	0	0
2574	1	98	0	1	0	0
2575	1	98	0	1	0	0
2576	1	98	0	1	0	0
2577	1	98	0	1	1	0
2578	11	98	1	1	1	0
2579 FF	4B		0	1	1	0
2580	1	98	0	1	1	0
2581	1	98	0	1	1	0
2582	1	98	0	1	0	0
2583	0	98	0	1	0	0
2584	0	98	0	1	0	0
2585	0	98	0	1	0	0
2586	0	98	0	1	1	0
2587 0E		98	1	1	1	0
2588 FF	4B		0	1	1	0
2589	0	98	0	1	1	0
2590	0	98	0	1	1	0
2591	0	98	0	0	1	0
2592	0	98	0	0	1	0
2593	0	98	0	0	1	0
2594	0	98	0	0	1	0
2595	0	98	0	1	1	0
2596 0E		98	1	1	1	0
2597 FF	4B		0	1	1	0
2598	0	98	0	1	1	0
2599	0	98	0	1	1	0

2600	0	98	0	1	0	0
2601	1	98	0	1	0	0
2602	1	98	0	1	0	0
2603	1	98	0	1	0	0
2604	1	98	0	1	1	0
2605	11	98	1	1	1	0
2606 FF	4C		0	1	1	0
2607	1	98	0	1	1	0
2608	1	98	0	1	1	0
2609	1	98	0	1	0	0
2610	1	98	0	1	0	0
2611	1	98	0	1	0	0
2612	1	98	0	1	0	0
2613	1	98	0	1	1	0
2614	11	98	1	1	1	0
2615 FF	4C		0	1	1	0
2616	1	98	0	1	1	0
2617	1	98	0	1	1	0
2618	1	98	0	1	0	0
2619	1	98	0	1	0	0
2620	1	98	0	1	0	0
2621	1	98	0	1	0	0
2622	1	98	0	1	1	0
2623	11	98	1	1	1	0
2624 FF		42	0	1	1	0
2625	1	98	0	1	1	0
2626	1	98	0	1	1	0
2627	1	98	0	1	0	0
2628	8	98	0	1	0	0
2629	8	98	0	1	0	0
2630	8	98	0	1	0	0
2631	8	98	0	1	1	0
2632	16	98	1	1	1	0
2633 FF		42	0	1	1	0
2634	8	98	0	1	1	0
2635	8	98	0	1	1	0
2636	8	98	0	1	0	0
2637	8	98	0	1	0	0
2638	80	98	0	1	0	0
2639	80	98	0	1	0	0
2640	80	98	0	1	1	0
2641	20	98	1	1	1	0
2642 FF		42	0	1	1	0
2643	80	98	0	1	1	0
2644	80	98	0	1	1	0
2645	80	98	0	1	0	0
2646	80	98	0	1	0	0
2647	6	98	0	1	0	0
2648	6	98	0	1	0	0
2649	6	98	0	1	1	0
2650	20	98	1	1	1	0
2651 FF		42	0	1	1	0

2652	6	98	0	1	1	0
2653	6	98	0	1	1	0
2654	6	98	0	1	0	0
2655	6	98	0	1	0	0
2656	0	98	0	1	0	0
2657	0	98	0	1	0	0
2658	0	98	0	1	1	0
2659	20	98	1	1	1	0
2660 FF		42	0	1	1	0
2661	0	98	0	1	1	0
2662	0	98	0	1	1	0
2663	0	98	0	1	0	0
2664	0	98	0	1	0	0
2665	3	98	0	1	0	0
2666	3	98	0	1	0	0
2667	3	98	0	1	1	0
2668	20	98	1	1	1	0
2669 FF		42	0	1	1	0
2670	3	98	0	1	1	0
2671	3	98	0	1	1	0
2672	3	98	0	1	0	0
2673	3	98	0	1	0	0
2674	0	98	0	1	0	0
2675	0	98	0	1	0	0
2676	0	98	0	1	1	0
2677	20	98	1	1	1	0
2678 FF		42	0	1	1	0
2679	0	98	0	1	1	0
2680	0	98	0	1	1	0
2681	0	98	0	1	0	0
2682	0	98	0	1	0	0
2683	0	98	0	1	0	0
2684	0	98	0	1	0	0
2685	0	98	0	1	1	0
2686	20	98	1	1	1	0
2687 FF		42	0	1	1	0
2688	0	98	0	1	1	0
2689	0	98	0	1	1	0
2690	0	98	0	1	0	0
2691	0	98	0	1	0	0
2692 FF		98	0	1	0	0
2693 FF		98	0	1	0	0
2694 FF		98	0	1	1	0
2695	20	98	1	1	1	0
2696 FF		42	0	1	1	0
2697 FF		98	0	1	1	0
2698 FF		98	0	1	1	0
2699 FF		98	0	1	0	0
2700 FF		98	0	1	0	0
2701	0	98	0	1	0	0
2702	0	98	0	1	0	0
2703	0	98	0	1	1	0

2704	20	98	1	1	1	0
2705 FF		42	0	1	1	0
2706	0	98	0	1	1	0
2707	0	98	0	1	1	0
2708	40	98	0	0	1	0
2709	40	98	0	0	1	0
2710	40	98	0	0	1	0
2711	40	98	0	0	1	0
2712	0	98	0	1	1	0
2713	11	98	1	1	1	0
2714 FF		42	0	1	1	0
2715	0	98	0	1	1	0
2716	0	98	0	1	1	0
2717	4	98	0	0	1	0
2718	4	98	0	0	1	0
2719	4	98	0	0	1	0
2720	4	98	0	0	1	0
2721	0	98	0	1	1	0
2722	20	98	1	1	1	0
2723 FF		48	0	1	1	0
2724	0	98	0	1	1	0
2725	0	98	0	1	1	0
2726	3	98	0	0	1	0
2727	3	98	0	0	1	0
2728	3	98	0	0	1	0
2729	3	98	0	0	1	0
2730	0	98	0	1	1	0
2731	20	98	1	1	1	0
2732 FF		48	0	1	1	0
2733	0	98	0	1	1	0
2734	0	98	0	1	1	0
2735	9	98	0	0	1	0
2736	9	98	0	0	1	0
2737	9	98	0	0	1	0
2738	9	98	0	0	1	0
2739	0	98	0	1	1	0
2740	20	98	1	1	1	0
2741 FF		48	0	1	1	0
2742	0	98	0	1	1	0
2743	0	98	0	1	1	0
2744	4	98	0	0	1	0
2745	4	98	0	0	1	0
2746	4	98	0	0	1	0
2747	4	98	0	0	1	0
2748	0	98	0	1	1	0
2749	20	98	1	1	1	0
2750 FF		48	0	1	1	0
2751	0	98	0	1	1	0
2752	0	98	0	1	1	0
2753 0A		98	0	0	1	0
2754 0A		98	0	0	1	0
2755 0A		98	0	0	1	0

2756	0A	98	0	0	1	0
2757	0	98	0	1	1	0
2758	11	98	1	1	1	0
2759	FF	48	0	1	1	0
2760	90	41	0	1	1	1
2761	A4	41	1	1	1	1
2762	90	41	0	1	1	1
2763	FF	5F	0	1	1	1
2764	41	41	0	1	1	1
2765	41	41	0	1	1	0
2766	0	98	0	1	1	0
2767	0	98	0	1	1	0
2768	0	98	0	1	0	0
2769	0	98	0	1	0	0
2770	0	98	0	1	0	0
2771	0	98	0	1	0	0
2772	0	98	0	1	1	0
2773	6	98	1	1	1	0
2774	FF	50	0	1	1	0
2775	0	98	0	1	1	0
2776	0	98	0	1	1	0
2777	0	98	0	1	0	0
2778	1	98	0	1	0	0
2779	1	98	0	1	0	0
2780	1	98	0	1	0	0
2781	1	98	0	1	1	0
2782	2	98	1	1	1	0
2783	FF	50	0	1	1	0
2784	1	98	0	1	1	0
2785	1	98	0	1	1	0
2786	1	98	0	1	0	0
2787	0	98	0	1	0	0
2788	0	98	0	1	0	0
2789	0	98	0	1	0	0
2790	0	98	0	1	1	0
2791	3	98	1	1	1	0
2792	FF	50	0	1	1	0
2793	0	98	0	1	1	0
2794	0	98	0	1	1	0
2795	0	98	0	1	0	0
2796	0	98	0	1	0	0
2797	0	98	0	1	0	0
2798	0	98	0	1	0	0
2799	0	98	0	1	1	0
2800	4	98	1	1	1	0
2801	FF	50	0	1	1	0
2802	0	98	0	1	1	0
2803	0	98	0	1	1	0
2804	0	98	0	1	0	0
2805	0	98	0	1	0	0
2806	0	98	0	1	0	0
2807	0	98	0	1	0	0

2808	0	98	0	1	1	0
2809	5	98	1	1	1	0
2810 FF		50	0	1	1	0
2811 E0		50	0	1	1	1
2812 7E		50	1	1	1	1
2813 E0		50	0	1	1	1
2814	3	50	0	1	1	1
2815	0	98	0	1	1	0
2816	0	98	0	1	1	0
2817	0	98	0	1	0	0
2818	0	98	0	1	0	0
2819	0	98	0	1	0	0
2820	0	98	0	1	0	0
2821	0	98	0	1	1	0
2822	11	98	1	1	1	0
2823 FF	4B		0	1	1	0
2824	0	98	0	1	1	0
2825	0	98	0	1	1	0
2826	0	98	0	1	0	0
2827	1	98	0	1	0	0
2828	1	98	0	1	0	0
2829	1	98	0	1	0	0
2830	1	98	0	1	1	0
2831	1	98	1	1	1	0
2832 FF	4B		0	1	1	0
2833	1	98	0	1	1	0
2834	1	98	0	1	1	0
2835	1	98	0	1	0	0
2836	0	98	0	1	0	0
2837	0	98	0	1	0	0
2838	0	98	0	1	0	0
2839	0	98	0	1	1	0
2840 0E		98	1	1	1	0
2841 FF	4B		0	1	1	0
2842	0	98	0	1	1	0
2843	0	98	0	1	1	0
2844	0	98	0	0	1	0
2845	0	98	0	0	1	0
2846	0	98	0	0	1	0
2847	0	98	0	0	1	0
2848	0	98	0	1	1	0
2849 0E		98	1	1	1	0
2850 FF	4B		0	1	1	0
2851	0	98	0	1	1	0
2852	0	98	0	1	1	0
2853	0	98	0	1	0	0
2854	0	98	0	1	0	0
2855	0	98	0	1	0	0
2856	0	98	0	1	0	0
2857	0	98	0	1	1	0
2858	11	98	1	1	1	0
2859 FF	4C		0	1	1	0

2860	0	98	0	1	1	0
2861	0	98	0	1	1	0
2862	0	98	0	1	0	0
2863	0	98	0	1	0	0
2864	0	98	0	1	0	0
2865	0	98	0	1	0	0
2866	0	98	0	1	1	0
2867	11	98	1	1	1	0
2868 FF	4C		0	1	1	0
2869	0	98	0	1	1	0
2870	0	98	0	1	1	0
2871	0	98	0	1	0	0
2872	0	98	0	1	0	0
2873	0	98	0	1	0	0
2874	0	98	0	1	0	0
2875	0	98	0	1	1	0
2876	11	98	1	1	1	0
2877 FF		42	0	1	1	0
2878	0	98	0	1	1	0
2879	0	98	0	1	1	0
2880	0	98	0	1	0	0
2881	0	98	0	1	0	0
2882	0	98	0	1	0	0
2883	0	98	0	1	0	0
2884	0	98	0	1	1	0
2885	6	98	1	1	1	0
2886 FF		50	0	1	1	0
2887	0	98	0	1	1	0
2888	0	98	0	1	1	0
2889	0	98	0	1	0	0
2890	1	98	0	1	0	0
2891	1	98	0	1	0	0
2892	1	98	0	1	0	0
2893	1	98	0	1	1	0
2894	2	98	1	1	1	0
2895 FF		50	0	1	1	0
2896	1	98	0	1	1	0
2897	1	98	0	1	1	0
2898	1	98	0	1	0	0
2899	0	98	0	1	0	0
2900	0	98	0	1	0	0
2901	0	98	0	1	0	0
2902	0	98	0	1	1	0
2903	3	98	1	1	1	0
2904 FF		50	0	1	1	0
2905	0	98	0	1	1	0
2906	0	98	0	1	1	0
2907	0	98	0	1	0	0
2908	0	98	0	1	0	0
2909	0	98	0	1	0	0
2910	0	98	0	1	0	0
2911	0	98	0	1	1	0

2912	4	98	1	1	1	0
2913 FF		50	0	1	1	0
2914	0	98	0	1	1	0
2915	0	98	0	1	1	0
2916	0	98	0	1	0	0
2917	0	98	0	1	0	0
2918	0	98	0	1	0	0
2919	0	98	0	1	0	0
2920	0	98	0	1	1	0
2921	5	98	1	1	1	0
2922 FF		50	0	1	1	0
2923	0	98	0	1	1	0
2924	0	98	0	1	1	0
2925	0	98	0	1	0	0
2926	0	98	0	1	0	0
2927	0	98	0	1	0	0
2928	0	98	0	1	0	0
2929	0	98	0	1	1	0
2930	11	98	1	1	1	0
2931 FF	4B		0	1	1	0
2932	0	98	0	1	1	0
2933	0	98	0	1	1	0
2934	0	98	0	1	0	0
2935	1	98	0	1	0	0
2936	1	98	0	1	0	0
2937	1	98	0	1	0	0
2938	1	98	0	1	1	0
2939	1	98	1	1	1	0
2940 FF	4B		0	1	1	0
2941	1	98	0	1	1	0
2942	1	98	0	1	1	0
2943	1	98	0	1	0	0
2944	0	98	0	1	0	0
2945	0	98	0	1	0	0
2946	0	98	0	1	0	0
2947	0	98	0	1	1	0
2948 0E		98	1	1	1	0
2949 FF	4B		0	1	1	0
2950	0	98	0	1	1	0
2951	0	98	0	1	1	0
2952	0	98	0	0	1	0
2953	0	98	0	0	1	0
2954	0	98	0	0	1	0
2955	0	98	0	0	1	0
2956	0	98	0	1	1	0
2957 0E		98	1	1	1	0
2958 FF	4B		0	1	1	0
2959	0	98	0	1	1	0
2960	0	98	0	1	1	0
2961	0	98	0	1	0	0
2962	0	98	0	1	0	0
2963	0	98	0	1	0	0

2964	0	98	0	1	0	0
2965	0	98	0	1	1	0
2966	11	98	1	1	1	0
2967 FF	4C		0	1	1	0
2968	0	98	0	1	1	0
2969	0	98	0	1	1	0
2970	0	98	0	1	0	0
2971	0	98	0	1	0	0
2972	0	98	0	1	0	0
2973	0	98	0	1	0	0
2974	0	98	0	1	1	0
2975	11	98	1	1	1	0
2976 FF	4C		0	1	1	0
2977	0	98	0	1	1	0
2978	0	98	0	1	1	0
2979	0	98	0	1	0	0
2980	0	98	0	1	0	0
2981	0	98	0	1	0	0
2982	0	98	0	1	0	0
2983	0	98	0	1	1	0
2984	11	98	1	1	1	0
2985 FF		42	0	1	1	0
2986	5	71	0	1	1	1
2987 3A		71	1	1	1	1
2988	5	71	0	1	1	1
2989 FF	7F		0	1	1	1
2990	5	71	0	1	1	1
2991	5	71	0	1	1	0
2992	0	98	0	1	1	0
2993	0	98	0	1	1	0
2994	0	98	0	1	0	0
2995	0	98	0	1	0	0
2996	0	98	0	1	0	0
2997	0	98	0	1	0	0
2998	0	98	0	1	1	0
2999	6	98	1	1	1	0
3000 FF		50	0	1	1	0
3001	0	98	0	1	1	0
3002	0	98	0	1	1	0
3003	0	98	0	1	0	0
3004	1	98	0	1	0	0
3005	1	98	0	1	0	0
3006	1	98	0	1	0	0
3007	1	98	0	1	1	0
3008	2	98	1	1	1	0
3009 FF		50	0	1	1	0
3010	1	98	0	1	1	0
3011	1	98	0	1	1	0
3012	1	98	0	1	0	0
3013	0	98	0	1	0	0
3014	0	98	0	1	0	0
3015	0	98	0	1	0	0

3016	0	98	0	1	1	0
3017	3	98	1	1	1	0
3018 FF		50	0	1	1	0
3019	0	98	0	1	1	0
3020	0	98	0	1	1	0
3021	0	98	0	1	0	0
3022	0	98	0	1	0	0
3023	0	98	0	1	0	0
3024	0	98	0	1	0	0
3025	0	98	0	1	1	0
3026	4	98	1	1	1	0
3027 FF		50	0	1	1	0
3028	0	98	0	1	1	0
3029	0	98	0	1	1	0
3030	0	98	0	1	0	0
3031	0	98	0	1	0	0
3032	0	98	0	1	0	0
3033	0	98	0	1	0	0
3034	0	98	0	1	1	0
3035	5	98	1	1	1	0
3036 FF		50	0	1	1	0
3037	0	98	0	1	1	0
3038	0	98	0	1	1	0
3039	0	98	0	1	0	0
3040	1	98	0	1	0	0
3041	1	98	0	1	0	0
3042	1	98	0	1	0	0
3043	1	98	0	1	1	0
3044	11	98	1	1	1	0
3045 FF	4B		0	1	1	0
3046	1	98	0	1	1	0
3047	1	98	0	1	1	0
3048	1	98	0	1	0	0
3049	0	98	0	1	0	0
3050	0	98	0	1	0	0
3051	0	98	0	1	0	0
3052	0	98	0	1	1	0
3053 0E		98	1	1	1	0
3054 FF	4B		0	1	1	0
3055	0	98	0	1	1	0
3056	0	98	0	1	1	0
3057	0	98	0	0	1	0
3058	0	98	0	0	1	0
3059	0	98	0	0	1	0
3060	0	98	0	0	1	0
3061	0	98	0	1	1	0
3062 0E		98	1	1	1	0
3063 FF	4B		0	1	1	0
3064	0	98	0	1	1	0
3065	0	98	0	1	1	0
3066	0	98	0	1	0	0
3067	1	98	0	1	0	0

3068	1	98	0	1	0	0
3069	1	98	0	1	0	0
3070	1	98	0	1	1	0
3071	11	98	1	1	1	0
3072 FF	4C		0	1	1	0
3073	1	98	0	1	1	0
3074	1	98	0	1	1	0
3075	1	98	0	1	0	0
3076	1	98	0	1	0	0
3077	1	98	0	1	0	0
3078	1	98	0	1	0	0
3079	1	98	0	1	1	0
3080	11	98	1	1	1	0
3081 FF	4C		0	1	1	0
3082	1	98	0	1	1	0
3083	1	98	0	1	1	0
3084	1	98	0	1	0	0
3085	1	98	0	1	0	0
3086	1	98	0	1	0	0
3087	1	98	0	1	0	0
3088	1	98	0	1	1	0
3089	11	98	1	1	1	0
3090 FF		42	0	1	1	0
3091	1	98	0	1	1	0
3092	1	98	0	1	1	0
3093	1	98	0	1	0	0
3094	8	98	0	1	0	0
3095	8	98	0	1	0	0
3096	8	98	0	1	0	0
3097	8	98	0	1	1	0
3098	16	98	1	1	1	0
3099 FF		42	0	1	1	0
3100	8	98	0	1	1	0
3101	8	98	0	1	1	0
3102	8	98	0	1	0	0
3103	8	98	0	1	0	0
3104	80	98	0	1	0	0
3105	80	98	0	1	0	0
3106	80	98	0	1	1	0
3107	20	98	1	1	1	0
3108 FF		42	0	1	1	0
3109	80	98	0	1	1	0
3110	80	98	0	1	1	0
3111	80	98	0	1	0	0
3112	80	98	0	1	0	0
3113	6	98	0	1	0	0
3114	6	98	0	1	0	0
3115	6	98	0	1	1	0
3116	20	98	1	1	1	0
3117 FF		42	0	1	1	0
3118	6	98	0	1	1	0
3119	6	98	0	1	1	0

3120	6	98	0	1	0	0
3121	6	98	0	1	0	0
3122	3	98	0	1	0	0
3123	3	98	0	1	0	0
3124	3	98	0	1	1	0
3125	20	98	1	1	1	0
3126 FF		42	0	1	1	0
3127	3	98	0	1	1	0
3128	3	98	0	1	1	0
3129	3	98	0	1	0	0
3130	3	98	0	1	0	0
3131	3	98	0	1	0	0
3132	3	98	0	1	0	0
3133	3	98	0	1	1	0
3134	20	98	1	1	1	0
3135 FF		42	0	1	1	0
3136	3	98	0	1	1	0
3137	3	98	0	1	1	0
3138	3	98	0	1	0	0
3139	3	98	0	1	0	0
3140	9	98	0	1	0	0
3141	9	98	0	1	0	0
3142	9	98	0	1	1	0
3143	20	98	1	1	1	0
3144 FF		42	0	1	1	0
3145	9	98	0	1	1	0
3146	9	98	0	1	1	0
3147	9	98	0	1	0	0
3148	9	98	0	1	0	0
3149	4	98	0	1	0	0
3150	4	98	0	1	0	0
3151	4	98	0	1	1	0
3152	20	98	1	1	1	0
3153 FF		42	0	1	1	0
3154	4	98	0	1	1	0
3155	4	98	0	1	1	0
3156	4	98	0	1	0	0
3157	4	98	0	1	0	0
3158 FF		98	0	1	0	0
3159 FF		98	0	1	0	0
3160 FF		98	0	1	1	0
3161	20	98	1	1	1	0
3162 FF		42	0	1	1	0
3163 FF		98	0	1	1	0
3164 FF		98	0	1	1	0
3165 FF		98	0	1	0	0
3166 FF		98	0	1	0	0
3167	0	98	0	1	0	0
3168	0	98	0	1	0	0
3169	0	98	0	1	1	0
3170	20	98	1	1	1	0
3171 FF		42	0	1	1	0

3172	0	98	0	1	1	0
3173	0	98	0	1	1	0
3174	40	98	0	0	1	0
3175	40	98	0	0	1	0
3176	40	98	0	0	1	0
3177	40	98	0	0	1	0
3178	0	98	0	1	1	0
3179	11	98	1	1	1	0
3180 FF		42	0	1	1	0
3181	0	98	0	1	1	0
3182	0	98	0	1	1	0
3183	66	98	0	0	1	0
3184	66	98	0	0	1	0
3185	66	98	0	0	1	0
3186	66	98	0	0	1	0
3187	0	98	0	1	1	0
3188	20	98	1	1	1	0
3189 FF		48	0	1	1	0
3190	0	98	0	1	1	0
3191	0	98	0	1	1	0
3192	3	98	0	0	1	0
3193	3	98	0	0	1	0
3194	3	98	0	0	1	0
3195	3	98	0	0	1	0
3196	0	98	0	1	1	0
3197	20	98	1	1	1	0
3198 FF		48	0	1	1	0
3199	0	98	0	1	1	0
3200	0	98	0	1	1	0
3201	53	98	0	0	1	0
3202	53	98	0	0	1	0
3203	53	98	0	0	1	0
3204	53	98	0	0	1	0
3205	0	98	0	1	1	0
3206	20	98	1	1	1	0
3207 FF		48	0	1	1	0
3208	0	98	0	1	1	0
3209	0	98	0	1	1	0
3210	0	98	0	0	1	0
3211	0	98	0	0	1	0
3212	0	98	0	0	1	0
3213	0	98	0	0	1	0
3214	0	98	0	1	1	0
3215	20	98	1	1	1	0
3216 FF		48	0	1	1	0
3217	0	98	0	1	1	0
3218	0	98	0	1	1	0
3219 2F		98	0	0	1	0
3220 2F		98	0	0	1	0
3221 2F		98	0	0	1	0
3222 2F		98	0	0	1	0
3223	0	98	0	1	1	0

3224	20	98	1	1	1	0
3225 FF		48	0	1	1	0
3226	0	98	0	1	1	0
3227	0	98	0	1	1	0
3228	0	98	0	0	1	0
3229	0	98	0	0	1	0
3230	0	98	0	0	1	0
3231	0	98	0	0	1	0
3232	0	98	0	1	1	0
3233	20	98	1	1	1	0
3234 FF		48	0	1	1	0
3235	0	98	0	1	1	0
3236	0	98	0	1	1	0
3237 4E		98	0	0	1	0
3238 4E		98	0	0	1	0
3239 4E		98	0	0	1	0
3240 4E		98	0	0	1	0
3241	0	98	0	1	1	0
3242	20	98	1	1	1	0
3243 FF		48	0	1	1	0
3244	0	98	0	1	1	0
3245	0	98	0	1	1	0
3246	0	98	0	0	1	0
3247	0	98	0	0	1	0
3248	0	98	0	0	1	0
3249	0	98	0	0	1	0
3250	0	98	0	1	1	0
3251	20	98	1	1	1	0
3252 FF		48	0	1	1	0
3253	0	98	0	1	1	0
3254	0	98	0	1	1	0
3255	2	98	0	0	1	0
3256	2	98	0	0	1	0
3257	2	98	0	0	1	0
3258	2	98	0	0	1	0
3259	0	98	0	1	1	0
3260	11	98	1	1	1	0
3261 FF		48	0	1	1	0
3262 D0		50	0	1	1	1
3263 B4		50	1	1	1	1
3264 D0		50	0	1	1	1
3265 D0		50	0	1	1	1
3266	0	98	0	1	1	0
3267	0	98	0	1	1	0
3268	0	98	0	1	0	0
3269	0	98	0	1	0	0
3270	0	98	0	1	0	0
3271	0	98	0	1	0	0
3272	0	98	0	1	1	0
3273	6	98	1	1	1	0
3274 FF		50	0	1	1	0
3275	0	98	0	1	1	0

3276	0	98	0	1	1	0
3277	0	98	0	1	0	0
3278	1	98	0	1	0	0
3279	1	98	0	1	0	0
3280	1	98	0	1	0	0
3281	1	98	0	1	1	0
3282	2	98	1	1	1	0
3283 FF		50	0	1	1	0
3284	1	98	0	1	1	0
3285	1	98	0	1	1	0
3286	1	98	0	1	0	0
3287	0	98	0	1	0	0
3288	0	98	0	1	0	0
3289	0	98	0	1	0	0
3290	0	98	0	1	1	0
3291	3	98	1	1	1	0
3292 FF		50	0	1	1	0
3293	0	98	0	1	1	0
3294	0	98	0	1	1	0
3295	0	98	0	1	0	0
3296	0	98	0	1	0	0
3297	0	98	0	1	0	0
3298	0	98	0	1	0	0
3299	0	98	0	1	1	0
3300	4	98	1	1	1	0
3301 FF		50	0	1	1	0
3302	0	98	0	1	1	0
3303	0	98	0	1	1	0
3304	0	98	0	1	0	0
3305	0	98	0	1	0	0
3306	0	98	0	1	0	0
3307	0	98	0	1	0	0
3308	0	98	0	1	1	0
3309	5	98	1	1	1	0
3310 FF		50	0	1	1	0
3311	0	98	0	1	1	0
3312	0	98	0	1	1	0
3313	0	98	0	1	0	0
3314	0	98	0	1	0	0
3315	0	98	0	1	0	0
3316	0	98	0	1	0	0
3317	0	98	0	1	1	0
3318	11	98	1	1	1	0
3319 FF	4B		0	1	1	0
3320	0	98	0	1	1	0
3321	0	98	0	1	1	0
3322	0	98	0	1	0	0
3323	1	98	0	1	0	0
3324	1	98	0	1	0	0
3325	1	98	0	1	0	0
3326	1	98	0	1	1	0
3327	1	98	1	1	1	0

3328	FF		4B		0	1	1	0
3329		1		98	0	1	1	0
3330		1		98	0	1	1	0
3331		1		98	0	1	0	0
3332		0		98	0	1	0	0
3333		0		98	0	1	0	0
3334		0		98	0	1	0	0
3335		0		98	0	1	1	0
3336	0E			98	1	1	1	0
3337	FF		4B		0	1	1	0
3338		0		98	0	1	1	0
3339		0		98	0	1	1	0
3340		0		98	0	0	1	0
3341		0		98	0	0	1	0
3342		0		98	0	0	1	0
3343		0		98	0	0	1	0
3344		0		98	0	1	1	0
3345	0E			98	1	1	1	0
3346	FF		4B		0	1	1	0
3347		0		98	0	1	1	0
3348		0		98	0	1	1	0
3349		0		98	0	1	0	0
3350		0		98	0	1	0	0
3351		0		98	0	1	0	0
3352		0		98	0	1	0	0
3353		0		98	0	1	1	0
3354		11		98	1	1	1	0
3355	FF		4C		0	1	1	0
3356		0		98	0	1	1	0
3357		0		98	0	1	1	0
3358		0		98	0	1	0	0
3359		0		98	0	1	0	0
3360		0		98	0	1	0	0
3361		0		98	0	1	0	0
3362		0		98	0	1	1	0
3363		11		98	1	1	1	0
3364	FF		4C		0	1	1	0
3365		0		98	0	1	1	0
3366		0		98	0	1	1	0
3367	3A			98	0	0	1	0
3368	3A			98	0	0	1	0
3369	3A			98	0	0	1	0
3370	3A			98	0	0	1	0
3371		0		98	0	1	1	0
3372		20		98	1	1	1	0
3373	FF			48	0	1	1	0
3374		0		98	0	1	1	0
3375		0		98	0	1	1	0
3376		0		98	0	0	1	0
3377		0		98	0	0	1	0
3378		0		98	0	0	1	0
3379		0		98	0	0	1	0

3380	0	98	0	1	1	0
3381	20	98	1	1	1	0
3382 FF		48	0	1	1	0
3383	0	98	0	1	1	0
3384	0	98	0	1	1	0
3385	62	98	0	0	1	0
3386	62	98	0	0	1	0
3387	62	98	0	0	1	0
3388	62	98	0	0	1	0
3389	0	98	0	1	1	0
3390	20	98	1	1	1	0
3391 FF		48	0	1	1	0
3392	0	98	0	1	1	0
3393	0	98	0	1	1	0
3394	0	98	0	0	1	0
3395	0	98	0	0	1	0
3396	0	98	0	0	1	0
3397	0	98	0	0	1	0
3398	0	98	0	1	1	0
3399	20	98	1	1	1	0
3400 FF		48	0	1	1	0
3401	0	98	0	1	1	0
3402	0	98	0	1	1	0
3403	33	98	0	0	1	0
3404	33	98	0	0	1	0
3405	33	98	0	0	1	0
3406	33	98	0	0	1	0
3407	0	98	0	1	1	0
3408	20	98	1	1	1	0
3409 FF		48	0	1	1	0
3410	0	98	0	1	1	0
3411	0	98	0	1	1	0
3412	0	98	0	0	1	0
3413	0	98	0	0	1	0
3414	0	98	0	0	1	0
3415	0	98	0	0	1	0
3416	0	98	0	1	1	0
3417	20	98	1	1	1	0
3418 FF		48	0	1	1	0
3419	0	98	0	1	1	0
3420	0	98	0	1	1	0
3421	62	98	0	0	1	0
3422	62	98	0	0	1	0
3423	62	98	0	0	1	0
3424	62	98	0	0	1	0
3425	0	98	0	1	1	0
3426	20	98	1	1	1	0
3427 FF		48	0	1	1	0
3428	0	98	0	1	1	0
3429	0	98	0	1	1	0
3430	0	98	0	0	1	0
3431	0	98	0	0	1	0

3432		0	98	0	0	1	0
3433		0	98	0	0	1	0
3434		0	98	0	1	1	0
3435		20	98	1	1	1	0
3436	FF		48	0	1	1	0
3437		0	98	0	1	1	0
3438		0	98	0	1	1	0
3439		2	98	0	0	1	0
3440		2	98	0	0	1	0
3441		2	98	0	0	1	0
3442		2	98	0	0	1	0
3443		0	98	0	1	1	0
3444		11	98	1	1	1	0
3445	FF		48	0	1	1	0
3446		12	3A	0	1	1	1
3447	3A		3A	0	1	1	1
3448	3A		3A	0	1	1	1
3449		49	3A	1	1	1	1
3450		0	98	0	1	1	0
3451		0	98	0	1	1	0
3452		0	98	0	1	0	0
3453		0	98	0	1	0	0
3454		0	98	0	1	0	0
3455		0	98	0	1	0	0
3456		0	98	0	1	1	0
3457		6	98	1	1	1	0
3458	FF		50	0	1	1	0
3459		0	98	0	1	1	0
3460		0	98	0	1	1	0
3461		0	98	0	1	0	0
3462		1	98	0	1	0	0
3463		1	98	0	1	0	0
3464		1	98	0	1	0	0
3465		1	98	0	1	1	0
3466		2	98	1	1	1	0
3467	FF		50	0	1	1	0
3468		1	98	0	1	1	0
3469		1	98	0	1	1	0
3470		1	98	0	1	0	0
3471		0	98	0	1	0	0
3472		0	98	0	1	0	0
3473		0	98	0	1	0	0
3474		0	98	0	1	1	0
3475		3	98	1	1	1	0
3476	FF		50	0	1	1	0
3477		0	98	0	1	1	0
3478		0	98	0	1	1	0
3479		0	98	0	1	0	0
3480		0	98	0	1	0	0
3481		0	98	0	1	0	0
3482		0	98	0	1	0	0
3483		0	98	0	1	1	0

3484	4	98	1	1	1	0
3485 FF		50	0	1	1	0
3486	0	98	0	1	1	0
3487	0	98	0	1	1	0
3488	0	98	0	1	0	0
3489	0	98	0	1	0	0
3490	0	98	0	1	0	0
3491	0	98	0	1	0	0
3492	0	98	0	1	1	0
3493	5	98	1	1	1	0
3494 FF		50	0	1	1	0
3495	0	98	0	1	1	0
3496	0	98	0	1	1	0
3497	0	98	0	1	0	0
3498	0	98	0	1	0	0
3499	0	98	0	1	0	0
3500	0	98	0	1	0	0
3501	0	98	0	1	1	0
3502	11	98	1	1	1	0
3503 FF	4B		0	1	1	0
3504	0	98	0	1	1	0
3505	0	98	0	1	1	0
3506	0	98	0	1	0	0
3507	1	98	0	1	0	0
3508	1	98	0	1	0	0
3509	1	98	0	1	0	0
3510	1	98	0	1	1	0
3511	1	98	1	1	1	0
3512 FF	4B		0	1	1	0
3513	1	98	0	1	1	0
3514	1	98	0	1	1	0
3515	1	98	0	1	0	0
3516	0	98	0	1	0	0
3517	0	98	0	1	0	0
3518	0	98	0	1	0	0
3519	0	98	0	1	1	0
3520 0E		98	1	1	1	0
3521 FF	4B		0	1	1	0
3522	0	98	0	1	1	0
3523	0	98	0	1	1	0
3524	0	98	0	0	1	0
3525	0	98	0	0	1	0
3526	0	98	0	0	1	0
3527	0	98	0	0	1	0
3528	0	98	0	1	1	0
3529 0E		98	1	1	1	0
3530 FF	4B		0	1	1	0
3531	0	98	0	1	1	0
3532	0	98	0	1	1	0
3533	0	98	0	1	0	0
3534	0	98	0	1	0	0
3535	0	98	0	1	0	0

3536	0	98	0	1	0	0
3537	0	98	0	1	1	0
3538	11	98	1	1	1	0
3539 FF	4C		0	1	1	0
3540	0	98	0	1	1	0
3541	0	98	0	1	1	0
3542	0	98	0	1	0	0
3543	0	98	0	1	0	0
3544	0	98	0	1	0	0
3545	0	98	0	1	0	0
3546	0	98	0	1	1	0
3547	11	98	1	1	1	0
3548 FF	4C		0	1	1	0
3549	0	98	0	1	1	0
3550	0	98	0	1	1	0
3551	34	98	0	0	1	0
3552	34	98	0	0	1	0
3553	34	98	0	0	1	0
3554	34	98	0	0	1	0
3555	0	98	0	1	1	0
3556	20	98	1	1	1	0
3557 FF		48	0	1	1	0
3558	0	98	0	1	1	0
3559	0	98	0	1	1	0
3560	0	98	0	0	1	0
3561	0	98	0	0	1	0
3562	0	98	0	0	1	0
3563	0	98	0	0	1	0
3564	0	98	0	1	1	0
3565	20	98	1	1	1	0
3566 FF		48	0	1	1	0
3567	0	98	0	1	1	0
3568	0	98	0	1	1	0
3569	39	98	0	0	1	0
3570	39	98	0	0	1	0
3571	39	98	0	0	1	0
3572	39	98	0	0	1	0
3573	0	98	0	1	1	0
3574	20	98	1	1	1	0
3575 FF		48	0	1	1	0
3576	0	98	0	1	1	0
3577	0	98	0	1	1	0
3578	0	98	0	0	1	0
3579	0	98	0	0	1	0
3580	0	98	0	0	1	0
3581	0	98	0	0	1	0
3582	0	98	0	1	1	0
3583	20	98	1	1	1	0
3584 FF		48	0	1	1	0
3585	0	98	0	1	1	0
3586	0	98	0	1	1	0
3587	35	98	0	0	1	0

3588	35	98	0	0	1	0
3589	35	98	0	0	1	0
3590	35	98	0	0	1	0
3591	0	98	0	1	1	0
3592	20	98	1	1	1	0
3593 FF		48	0	1	1	0
3594	0	98	0	1	1	0
3595	0	98	0	1	1	0
3596	0	98	0	0	1	0
3597	0	98	0	0	1	0
3598	0	98	0	0	1	0
3599	0	98	0	0	1	0
3600	0	98	0	1	1	0
3601	20	98	1	1	1	0
3602 FF		48	0	1	1	0
3603	0	98	0	1	1	0
3604	0	98	0	1	1	0
3605	37	98	0	0	1	0
3606	37	98	0	0	1	0
3607	37	98	0	0	1	0
3608	37	98	0	0	1	0
3609	0	98	0	1	1	0
3610	20	98	1	1	1	0
3611 FF		48	0	1	1	0
3612	0	98	0	1	1	0
3613	0	98	0	1	1	0
3614	0	98	0	0	1	0
3615	0	98	0	0	1	0
3616	0	98	0	0	1	0
3617	0	98	0	0	1	0
3618	0	98	0	1	1	0
3619	20	98	1	1	1	0
3620 FF		48	0	1	1	0
3621	0	98	0	1	1	0
3622	0	98	0	1	1	0
3623	2	98	0	0	1	0
3624	2	98	0	0	1	0
3625	2	98	0	0	1	0
3626	2	98	0	0	1	0
3627	0	98	0	1	1	0
3628	11	98	1	1	1	0
3629 FF		48	0	1	1	0
3630	7 3A		0	1	1	1
3631	78 3A		0	1	1	1
3632	78 3A		0	1	1	1
3633	50 3A		1	1	1	1
3634	0	98	0	1	1	0
3635	0	98	0	1	1	0
3636	0	98	0	1	0	0
3637	0	98	0	1	0	0
3638	0	98	0	1	0	0
3639	0	98	0	1	0	0

3640	0	98	0	1	1	0
3641	6	98	1	1	1	0
3642 FF		50	0	1	1	0
3643	0	98	0	1	1	0
3644	0	98	0	1	1	0
3645	0	98	0	1	0	0
3646	1	98	0	1	0	0
3647	1	98	0	1	0	0
3648	1	98	0	1	0	0
3649	1	98	0	1	1	0
3650	2	98	1	1	1	0
3651 FF		50	0	1	1	0
3652	1	98	0	1	1	0
3653	1	98	0	1	1	0
3654	1	98	0	1	0	0
3655	0	98	0	1	0	0
3656	0	98	0	1	0	0
3657	0	98	0	1	0	0
3658	0	98	0	1	1	0
3659	3	98	1	1	1	0
3660 FF		50	0	1	1	0
3661	0	98	0	1	1	0
3662	0	98	0	1	1	0
3663	0	98	0	1	0	0
3664	0	98	0	1	0	0
3665	0	98	0	1	0	0
3666	0	98	0	1	0	0
3667	0	98	0	1	1	0
3668	4	98	1	1	1	0
3669 FF		50	0	1	1	0
3670	0	98	0	1	1	0
3671	0	98	0	1	1	0
3672	0	98	0	1	0	0
3673	0	98	0	1	0	0
3674	0	98	0	1	0	0
3675	0	98	0	1	0	0
3676	0	98	0	1	1	0
3677	5	98	1	1	1	0
3678 FF		50	0	1	1	0
3679	0	98	0	1	1	0
3680	0	98	0	1	1	0
3681	0	98	0	1	0	0
3682	0	98	0	1	0	0
3683	0	98	0	1	0	0
3684	0	98	0	1	0	0
3685	0	98	0	1	1	0
3686	11	98	1	1	1	0
3687 FF	4B		0	1	1	0
3688	0	98	0	1	1	0
3689	0	98	0	1	1	0
3690	0	98	0	1	0	0
3691	1	98	0	1	0	0

3692	1	98	0	1	0	0
3693	1	98	0	1	0	0
3694	1	98	0	1	1	0
3695	1	98	1	1	1	0
3696 FF	4B		0	1	1	0
3697	1	98	0	1	1	0
3698	1	98	0	1	1	0
3699	1	98	0	1	0	0
3700	0	98	0	1	0	0
3701	0	98	0	1	0	0
3702	0	98	0	1	0	0
3703	0	98	0	1	1	0
3704 0E		98	1	1	1	0
3705 FF	4B		0	1	1	0
3706	0	98	0	1	1	0
3707	0	98	0	1	1	0
3708	0	98	0	0	1	0
3709	0	98	0	0	1	0
3710	0	98	0	0	1	0
3711	0	98	0	0	1	0
3712	0	98	0	1	1	0
3713 0E		98	1	1	1	0
3714 FF	4B		0	1	1	0
3715	0	98	0	1	1	0
3716	0	98	0	1	1	0
3717	0	98	0	1	0	0
3718	0	98	0	1	0	0
3719	0	98	0	1	0	0
3720	0	98	0	1	0	0
3721	0	98	0	1	1	0
3722	11	98	1	1	1	0
3723 FF	4C		0	1	1	0
3724	0	98	0	1	1	0
3725	0	98	0	1	1	0
3726	0	98	0	1	0	0
3727	0	98	0	1	0	0
3728	0	98	0	1	0	0
3729	0	98	0	1	0	0
3730	0	98	0	1	1	0
3731	11	98	1	1	1	0
3732 FF	4C		0	1	1	0
3733	0	98	0	1	1	0
3734	0	98	0	1	1	0
3735	36	98	0	0	1	0
3736	36	98	0	0	1	0
3737	36	98	0	0	1	0
3738	36	98	0	0	1	0
3739	0	98	0	1	1	0
3740	20	98	1	1	1	0
3741 FF		48	0	1	1	0
3742	0	98	0	1	1	0
3743	0	98	0	1	1	0

3744	0	98	0	0	1	0
3745	0	98	0	0	1	0
3746	0	98	0	0	1	0
3747	0	98	0	0	1	0
3748	0	98	0	1	1	0
3749	20	98	1	1	1	0
3750 FF		48	0	1	1	0
3751	0	98	0	1	1	0
3752	0	98	0	1	1	0
3753	66	98	0	0	1	0
3754	66	98	0	0	1	0
3755	66	98	0	0	1	0
3756	66	98	0	0	1	0
3757	0	98	0	1	1	0
3758	20	98	1	1	1	0
3759 FF		48	0	1	1	0
3760	0	98	0	1	1	0
3761	0	98	0	1	1	0
3762	0	98	0	0	1	0
3763	0	98	0	0	1	0
3764	0	98	0	0	1	0
3765	0	98	0	0	1	0
3766	0	98	0	1	1	0
3767	20	98	1	1	1	0
3768 FF		48	0	1	1	0
3769	0	98	0	1	1	0
3770	0	98	0	1	1	0
3771	32	98	0	0	1	0
3772	32	98	0	0	1	0
3773	32	98	0	0	1	0
3774	32	98	0	0	1	0
3775	0	98	0	1	1	0
3776	20	98	1	1	1	0
3777 FF		48	0	1	1	0
3778	0	98	0	1	1	0
3779	0	98	0	1	1	0
3780	0	98	0	0	1	0
3781	0	98	0	0	1	0
3782	0	98	0	0	1	0
3783	0	98	0	0	1	0
3784	0	98	0	1	1	0
3785	20	98	1	1	1	0
3786 FF		48	0	1	1	0
3787	0	98	0	1	1	0
3788	0	98	0	1	1	0
3789	62	98	0	0	1	0
3790	62	98	0	0	1	0
3791	62	98	0	0	1	0
3792	62	98	0	0	1	0
3793	0	98	0	1	1	0
3794	20	98	1	1	1	0
3795 FF		48	0	1	1	0

3796	0	98	0	1	1	0
3797	0	98	0	1	1	0
3798	0	98	0	0	1	0
3799	0	98	0	0	1	0
3800	0	98	0	0	1	0
3801	0	98	0	0	1	0
3802	0	98	0	1	1	0
3803	20	98	1	1	1	0
3804 FF		48	0	1	1	0
3805	0	98	0	1	1	0
3806	0	98	0	1	1	0
3807	2	98	0	0	1	0
3808	2	98	0	0	1	0
3809	2	98	0	0	1	0
3810	2	98	0	0	1	0
3811	0	98	0	1	1	0
3812	11	98	1	1	1	0
3813 FF		48	0	1	1	0
3814 D0		50	0	1	1	1
3815 F0		50	0	1	1	1
3816 F0		50	0	1	1	1
3817 BA		50	1	1	1	1
3818	0	98	0	1	1	0
3819	0	98	0	1	1	0
3820	0	98	0	1	0	0
3821	0	98	0	1	0	0
3822	0	98	0	1	0	0
3823	0	98	0	1	0	0
3824	0	98	0	1	1	0
3825	6	98	1	1	1	0
3826 FF		50	0	1	1	0
3827	0	98	0	1	1	0
3828	0	98	0	1	1	0
3829	0	98	0	1	0	0
3830	1	98	0	1	0	0
3831	1	98	0	1	0	0
3832	1	98	0	1	0	0
3833	1	98	0	1	1	0
3834	2	98	1	1	1	0
3835 FF		50	0	1	1	0
3836	1	98	0	1	1	0
3837	1	98	0	1	1	0
3838	1	98	0	1	0	0
3839	0	98	0	1	0	0
3840	0	98	0	1	0	0
3841	0	98	0	1	0	0
3842	0	98	0	1	1	0
3843	3	98	1	1	1	0
3844 FF		50	0	1	1	0
3845	0	98	0	1	1	0
3846	0	98	0	1	1	0
3847	0	98	0	1	0	0

3848	0	98	0	1	0	0
3849	0	98	0	1	0	0
3850	0	98	0	1	0	0
3851	0	98	0	1	1	0
3852	4	98	1	1	1	0
3853 FF		50	0	1	1	0
3854	0	98	0	1	1	0
3855	0	98	0	1	1	0
3856	0	98	0	1	0	0
3857	0	98	0	1	0	0
3858	0	98	0	1	0	0
3859	0	98	0	1	0	0
3860	0	98	0	1	1	0
3861	5	98	1	1	1	0
3862 FF		50	0	1	1	0
3863	0	98	0	1	1	0
3864	0	98	0	1	1	0
3865	0	98	0	1	0	0
3866	0	98	0	1	0	0
3867	0	98	0	1	0	0
3868	0	98	0	1	0	0
3869	0	98	0	1	1	0
3870	11	98	1	1	1	0
3871 FF	4B		0	1	1	0
3872	0	98	0	1	1	0
3873	0	98	0	1	1	0
3874	0	98	0	1	0	0
3875	1	98	0	1	0	0
3876	1	98	0	1	0	0
3877	1	98	0	1	0	0
3878	1	98	0	1	1	0
3879	1	98	1	1	1	0
3880 FF	4B		0	1	1	0
3881	1	98	0	1	1	0
3882	1	98	0	1	1	0
3883	1	98	0	1	0	0
3884	0	98	0	1	0	0
3885	0	98	0	1	0	0
3886	0	98	0	1	0	0
3887	0	98	0	1	1	0
3888 0E		98	1	1	1	0
3889 FF	4B		0	1	1	0
3890	0	98	0	1	1	0
3891	0	98	0	1	1	0
3892	0	98	0	0	1	0
3893	0	98	0	0	1	0
3894	0	98	0	0	1	0
3895	0	98	0	0	1	0
3896	0	98	0	1	1	0
3897 0E		98	1	1	1	0
3898 FF	4B		0	1	1	0
3899	0	98	0	1	1	0

3900	0	98	0	1	1	0
3901	0	98	0	1	0	0
3902	0	98	0	1	0	0
3903	0	98	0	1	0	0
3904	0	98	0	1	0	0
3905	0	98	0	1	1	0
3906	11	98	1	1	1	0
3907 FF	4C		0	1	1	0
3908	0	98	0	1	1	0
3909	0	98	0	1	1	0
3910	0	98	0	1	0	0
3911	0	98	0	1	0	0
3912	0	98	0	1	0	0
3913	0	98	0	1	0	0
3914	0	98	0	1	1	0
3915	11	98	1	1	1	0
3916 FF	4C		0	1	1	0
3917	0	98	0	1	1	0
3918	0	98	0	1	1	0
3919	62	98	0	0	1	0
3920	62	98	0	0	1	0
3921	62	98	0	0	1	0
3922	62	98	0	0	1	0
3923	0	98	0	1	1	0
3924	20	98	1	1	1	0
3925 FF		48	0	1	1	0
3926	0	98	0	1	1	0
3927	0	98	0	1	1	0
3928	0	98	0	0	1	0
3929	0	98	0	0	1	0
3930	0	98	0	0	1	0
3931	0	98	0	0	1	0
3932	0	98	0	1	1	0
3933	20	98	1	1	1	0
3934 FF		48	0	1	1	0
3935	0	98	0	1	1	0
3936	0	98	0	1	1	0
3937	64	98	0	0	1	0
3938	64	98	0	0	1	0
3939	64	98	0	0	1	0
3940	64	98	0	0	1	0
3941	0	98	0	1	1	0
3942	20	98	1	1	1	0
3943 FF		48	0	1	1	0
3944	0	98	0	1	1	0
3945	0	98	0	1	1	0
3946	0	98	0	0	1	0
3947	0	98	0	0	1	0
3948	0	98	0	0	1	0
3949	0	98	0	0	1	0
3950	0	98	0	1	1	0
3951	20	98	1	1	1	0

3952	FF		48	0	1	1	0
3953		0	98	0	1	1	0
3954		0	98	0	1	1	0
3955		35	98	0	0	1	0
3956		35	98	0	0	1	0
3957		35	98	0	0	1	0
3958		35	98	0	0	1	0
3959		0	98	0	1	1	0
3960		20	98	1	1	1	0
3961	FF		48	0	1	1	0
3962		0	98	0	1	1	0
3963		0	98	0	1	1	0
3964		0	98	0	0	1	0
3965		0	98	0	0	1	0
3966		0	98	0	0	1	0
3967		0	98	0	0	1	0
3968		0	98	0	1	1	0
3969		20	98	1	1	1	0
3970	FF		48	0	1	1	0
3971		0	98	0	1	1	0
3972		0	98	0	1	1	0
3973		31	98	0	0	1	0
3974		31	98	0	0	1	0
3975		31	98	0	0	1	0
3976		31	98	0	0	1	0
3977		0	98	0	1	1	0
3978		20	98	1	1	1	0
3979	FF		48	0	1	1	0
3980		0	98	0	1	1	0
3981		0	98	0	1	1	0
3982		0	98	0	0	1	0
3983		0	98	0	0	1	0
3984		0	98	0	0	1	0
3985		0	98	0	0	1	0
3986		0	98	0	1	1	0
3987		20	98	1	1	1	0
3988	FF		48	0	1	1	0
3989		0	98	0	1	1	0
3990		0	98	0	1	1	0
3991		2	98	0	0	1	0
3992		2	98	0	0	1	0
3993		2	98	0	0	1	0
3994		2	98	0	0	1	0
3995		0	98	0	1	1	0
3996		11	98	1	1	1	0
3997	FF		48	0	1	1	0
3998	A9	3A		0	1	1	1
3999	FF	7F		0	1	1	1
4000		2 3A		0	1	1	1
4001		2 3A		0	1	1	1
4002	A2	3A		1	1	1	1
4003		2	70	0	1	1	0

4004	0	98	0	1	1	0
4005	0	98	0	1	1	0
4006	0	98	0	1	0	0
4007	0	98	0	1	0	0
4008	0	98	0	1	0	0
4009	0	98	0	1	0	0
4010	0	98	0	1	1	0
4011	6	98	1	1	1	0
4012 FF		50	0	1	1	0
4013	0	98	0	1	1	0
4014	0	98	0	1	1	0
4015	0	98	0	1	0	0
4016	1	98	0	1	0	0
4017	1	98	0	1	0	0
4018	1	98	0	1	0	0
4019	1	98	0	1	1	0
4020	2	98	1	1	1	0
4021 FF		50	0	1	1	0
4022	1	98	0	1	1	0
4023	1	98	0	1	1	0
4024	1	98	0	1	0	0
4025	0	98	0	1	0	0
4026	0	98	0	1	0	0
4027	0	98	0	1	0	0
4028	0	98	0	1	1	0
4029	3	98	1	1	1	0
4030 FF		50	0	1	1	0
4031	0	98	0	1	1	0
4032	0	98	0	1	1	0
4033	0	98	0	1	0	0
4034	0	98	0	1	0	0
4035	0	98	0	1	0	0
4036	0	98	0	1	0	0
4037	0	98	0	1	1	0
4038	4	98	1	1	1	0
4039 FF		50	0	1	1	0
4040	0	98	0	1	1	0
4041	0	98	0	1	1	0
4042	0	98	0	1	0	0
4043	0	98	0	1	0	0
4044	0	98	0	1	0	0
4045	0	98	0	1	0	0
4046	0	98	0	1	1	0
4047	5	98	1	1	1	0
4048 FF		50	0	1	1	0
4049	0	98	0	1	1	0
4050	0	98	0	1	1	0
4051	0	98	0	1	0	0
4052	0	98	0	1	0	0
4053	0	98	0	1	0	0
4054	0	98	0	1	0	0
4055	0	98	0	1	1	0

4056	11	98	1	1	1	0
4057 FF	4B		0	1	1	0
4058	0	98	0	1	1	0
4059	0	98	0	1	1	0
4060	0	98	0	1	0	0
4061	1	98	0	1	0	0
4062	1	98	0	1	0	0
4063	1	98	0	1	0	0
4064	1	98	0	1	1	0
4065	1	98	1	1	1	0
4066 FF	4B		0	1	1	0
4067	1	98	0	1	1	0
4068	1	98	0	1	1	0
4069	1	98	0	1	0	0
4070	0	98	0	1	0	0
4071	0	98	0	1	0	0
4072	0	98	0	1	0	0
4073	0	98	0	1	1	0
4074 0E		98	1	1	1	0
4075 FF	4B		0	1	1	0
4076	0	98	0	1	1	0
4077	0	98	0	1	1	0
4078	0	98	0	0	1	0
4079	0	98	0	0	1	0
4080	0	98	0	0	1	0
4081	0	98	0	0	1	0
4082	0	98	0	1	1	0
4083 0E		98	1	1	1	0
4084 FF	4B		0	1	1	0
4085	0	98	0	1	1	0
4086	0	98	0	1	1	0
4087	0	98	0	1	0	0
4088	0	98	0	1	0	0
4089	0	98	0	1	0	0
4090	0	98	0	1	0	0
4091	0	98	0	1	1	0
4092	11	98	1	1	1	0
4093 FF	4C		0	1	1	0
4094	0	98	0	1	1	0
4095	0	98	0	1	1	0

Time Printed: 10 Oct 15 :06 :07

n

nterrupt

!USB, no int set

!IN1, endpoint 0 int set

!IN2, no int set

!OUT1, no int set

!OUT2, no int set

nterrupt

0, SetupEnd is set

er, nothing set

er, set Enable Suspend

x, nothing set

x, set to 0

0, SetupEnd is set

0, SetupEnd is set

0, clear SetupEnd and set ServiceSetupEnc

0, nothing set

!USB, nothing set

!IN1, EPO is set

!IN2, nothing set

!OUT1, nothing set

!OUT2, nothing set

0, nothing is set

er, Enable Suspend is set

x, set to 0

x, set to 0

0, nothing set

0, nothing set

0, nothing set

nterrupt

ISB, Reset is set

IN1, nothing set

IN2, nothing set

OUT1, nothing set

?OUT2, nothing set

DR, set to 0

DR, set to 0

?IN1E, Set to 0

?IN2E, Set to 0

?OUT1E, Set to 0

?OUT2E, Set to 0

?IN1E, Set to 0

?IN1E, set EPO

ISBE, set Reset, Resume, Suspend

nterrupt

?USB, nothing set

?IN1, EPO is set

!IN2, nothing set

!OUT1, nothing set

!OUT2, nothing set

0, OutPktRdy is set

x, set to 0

x, set to 0

0, OutPktRdy is set

0, OutPktRdy is set

0, OutPktRdy is set

nt0, set to 8

data is 0

data is 5

data is 2

data is 0

data is 0

data is 0

data is 0

data is 0

0, set Serviced OutPktRdy, DataEnd

nterrupt

USB, nothing set

IN1, EP0 is set

IN2, nothing set

!OUT1, nothing set

!OUT2, nothing set

0, nothing set

er, nothing set ?

er, set Suspend Enable

DR, set to 0

FADDR, set to 2

x, set to 0

x, set to 0

0, nothing set

0, nothing set

0, nothing set

iterrupt

!IN1, EP0 is set

0, OutPktRdy is set

x to 0

0, OutPktRdy is set

0, OutPktRdy is set

0, OutPktRdy is set

INT0, set to 8

Data is 80

Data is 06

Data is 0

Data is 1

Data is 0

Data is 0

Data is 12

Data is 0

0, set Serviced OutPktRdy

Data = 12

Data = 1

Data = 10

Data = 1

Data = 0

Data = 0

Data = 0

Data = 8

:SR0, set InPktRdy Send Descr

ıterrupt

!IN1, EPO interrupt set

0, nothing set

er, Enable suspend is set

x, Index = 0

x, set to 0

0, nothing set

0, nothing set

Data = E0

Data = 5

Data = 0

Data = 2

Data = 0

Data = 3

Data = 1

Data = 2

0, set InPktRdy

terrupt

!IN1, EPO interrupt is set

0, nothing is set

er, Suspend enabled

$x = 0$

$x = 0$

$0 = 0$

$0 = 0$

= 3

= 1

0, set data end and InPktRdy

terrupt

IN1, EP0 is set

0, nothing is set

er, Suspend enabled

x = 0

x = 0

0, nothing is set

0, nothing is set

0, nothing is set

interrupt

IN1, EP0 is set

0, OutPktRdy

x = 0

x = 0

0, OutPktRdy

0, OutPktRdy

0, OutPktRdy

COUNT1 = 8

data = 80

data = 6

data = 0

data = 2

Data = 0

data = 0

data = 9

data = 0

0, Set ServicedOutPktRdy

0, set InPktRdy

interrupt

EXHIBIT P

Symbol-UTMC Digital Netlist Hand-off Checklist

The following augments the Design Transfer Checklist (Appendix C) of the Mixed-Signal ASIC Digital Section Design Checklist.

Assumptions:

1. Symbol will do all digital design.
2. Symbol will do synthesis and timing using
   lgs035sc3_max(min).db
   fbl035lgs035_sc_max(min).vhd (Static Timing)

   Symbol could not simulate using the SDF file generated by the Synopsys tools.

3. Symbol will insert scan.

   UTMC will insert scan

4. Symbol will write/produce all sign-off testbenches and test vectors (if applicable).

Checklist:

_X__ VHDL gate netlist.
Netlist file name: __MULTITOP.vhd_____
Top level digital module name __MULTITOP_____
___ SDF file name:__none_____
yes_ Are all testbenches run with results validated, or "passed" indicated?
no_ Are all testbenches run with pre-route SDF timing files?
yes_ Are instructions for running the testbenches included?
no_ Are there any simulation warnings, and their reports included?

All warnings are in regard to the UTMC RAMs used with the USB core.

yes Final Synopsys Area report: _____ sq microns

Sent 4/3/01 in report file.

yes Clock(s) and timing specifications included.

```
/* This should be a list of all legal clock names in the design */
legal_clocks = {"CLK_CPU","FCLK","CLK_IN_PLL", "WR", "WR_N"}

/* Each clock has an associated parameter list */
```

```
/* Actual FCLK frequency is 48 MHz */
FCLK_period = 20
FCLK_waveform = "{0 10}"
FCLK_skew = 0.500
FCLK_input_delay = 2
FCLK_output_delay = 1.5


/* Actual CLK_IN_PLL frequency is 48 MHz */
CLK_IN_PLL_period = 20
CLK_IN_PLL_waveform = "{0 10}"
CLK_IN_PLL_skew = 0.500
CLK_IN_PLL_input_delay = 2
CLK_IN_PLL_output_delay = 1.5


/* Actual CLK_CPU frequency is 24 MHz */
CLK_CPU_period = 40
CLK_CPU_waveform = "{0 20}"
CLK_CPU_skew = 0.500
CLK_CPU_input_delay = 2
CLK_CPU_output_delay = 1.5


/* Actual WR frequency is 12 MHz */
WR_period = 80
WR_waveform = "{0 40}"
WR_skew = 0.500
WR_input_delay = 2
WR_output_delay = 1.5

/* Actual WR_N frequency is 12 MHz */
WR_N_period = 80
WR_N_waveform = "{0 40}"
WR_N_skew = 0.500
WR_N_input_delay = 2
WR_N_output_delay = 1.5

/* A virtual clock is used for purely combinational designs */
/* If no other clock is present, a virtual clock called VCLK will be
created */
Virtual_clk_period = 20
Virtual_clk_waveform = "{0 10}"
Virtual_clk_skew = 0.500
Virtual_clk_input_delay = 2
Virtual_clk_output_delay = 1.5
```

Deliverables:

1. This is to be the VHDL gate netlist of top level design. **Top Level** module should consists only of instantiations of the three types of hierarchical design modules: **top level digital**, **IOs**, and/or **Analog** modules. The **IOs** and **Analog** modules could be empty modules, or blocks representing "modeled" analog functionalities, or containing instantiations of actual IO cells.

2. The pre-route SDF file for **Top Level**, or **top level digital** module that was used with the provided testbenches should be included.
3. Provide VHDL testbenches that instantiate the **Top Level** or **top level digital**, which ever is applicable. The same testbenches will be simulated after place & route and used as post route sign-off criteria. It is up to Symbol to ensure that the testbenches provide adequate functionality and/or fault coverage to satisfy design hand-off. Testbenches and results/vectors can be in any format, however they must be simulator independent. Instructions or scripts to run and compare results would be very helpful. Also logs of any warnings would also help facilitates validation of database.
4. Timing specifications: A text document specifying clock requirements (required), input/output timing requirements (optional), and critical paths specifications (optional) shall be provided.
5. Synopsys area report (or the actual synopsys *.db database of the synthesized design from which we can generate area reports).

After Place & Route, UTMC will provide a flatten VHDL gate netlist and a corresponding SDF backannotated timing files of the **top level digital**.

EXHIBIT Q

Interrupt Scheme

INT0_N: Active low, configurable as edge or level sensitive.

INT1_N: Active low, configurable as edge or level sensitive.

INT2: Active high, edge sensitive.

INT5_N: Active low, edge sensitive.

INT0_N gets a low level when there is a WAKEUP condition or the WDT has expired.

INT1_N gets a low level when the 8051's transmit mailbox is empty or it's receive mailbox is full.

INT2 gets a 160 ns pulse (active high) when the OCIA transmit register is empty or Or the OCIA receive register is full, or when there is an USB interrupt.

Note: OCIA and USB are mutually exclusive.

INT5_N gets an 160 ns pulse (active low) when the SOF_PULSE is active or When the DMA finishes a transfer.

Mechanics

WAKEUP interrupt:

- Before going to sleep, enable the appropriate mask bits in the Wakeup control register.
- When an interrupt occurs, read the Interrupt control register (optional).
- Then read the Wakeup status register to determine what caused the wakeup
- To clear the interrupt, write a '1' to the status register bit that is set.

WDT interrupt:

- Enable the WDT mask bits in the WDT control/status register.
- When an interrupt occurs, read the Interrupt control register (optional).
- Then read the WDT control/status register to determine if a WDT interrupt. occurred.
- The interrupt gets cleared on the read.

Mailboxes interrupt:

- Enable the appropriate mask bits in the mailbox interrupt control register.
- When an interrupt occurs, read the Interrupt control register (optional).
- Then read the mailbox interrupt status register to determine what caused the interrupt.
- If the interrupt was caused by a the mailbox being read (empty), then to clear the interrupt, write a '1' to bit 6 of the mailbox interrupt status register. If the mailbox being filled caused the interrupt, then to clear the interrupt, read mailbox register 7.

OCIA interrupt:

- Enable the appropriate mask bits in the OCIA control register.
- When an interrupt occurs, read the Interrupt control register (optional).
- Then read the OCIA status register to determine what caused the interrupt
- Reading of the status will clear the interrupt.

USB interrupt:

- Enable the appropriate mask bits in the USB core.
- When an interrupt occurs, read the Interrupt control register (optional).
- Then read to a USB register to determine what caused the interrupt.
- To clear the interrupt see TONY.

DMA interrupt:

- Enable the mask bit in the DMA control register.
- When an interrupt occurs, read the Interrupt control register.
- To clear the interrupt, write a '1' to bit 0 of the Interrupt Control register.

SOF interrupt:

- Enable mask bit 5 in the Interrupt mask register.
- When an interrupt occurs, read the Interrupt control register.
- To clear the interrupt, write a '1' to bit 5 of the Interrupt Control register.

Vendor Selection Process

- Criteria
  - Vendor must have a process that can accommodate high speed digital logic and the RS232 charge pumps.
  - Piece price in $2 range for a volume of 1 million.
  - Turn-key design

Vendor Selection Process

- Ask for quotes from:
  - STMicro, Cypress, AMI, TI
  - VLSI, Atmel, Alcatel, UTMC
  - Fujitsu, Rohm, Epson, Maxim
  - Mitel
- Everyone except Alcatel and UTMC no bid due to RS232/USB requirement

Vendor Selection Process

- UTMC
  - Fab-less, not an approved vendor
  - Initially quoted: 64 pin [redacted]
    - NRE : $ 200,000
    - Placement of a 500K piece production order
    - 26 weeks to protos, 12 weeks for production
    - $2.78 @ 500K/year, $2.67 @ 1M/year

Vendor Selection Process

- Alcatel
  - Not an approved vendor
  - Quoted: 64 pin TQFP
    - NRE : $238,000
      - Re-spin: Free, if device does not meet spec.
    - 28 weeks to protos, 12 weeks for production
    - 2001: $2.09 @ 500K/year, $2.03 @ 1M/year
    - 2004: $1.91 @ 500K/year, $1.85 @ 1M/year

EXHIBIT S

Decoder memory map

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
00H	Mailbox 0	R								
01H	Mailbox 1	R								
02H	Mailbox 2	R								
03H	Mailbox 3	R								
04H	Mailbox 4	R								
05H	Mailbox 5	R								
06H	Mailbox 6	R								
07H	Mailbox 7	R								
00H	Mailbox 0	W								
01H	Mailbox 1	W								
02H	Mailbox 2	W								
03H	Mailbox 3	W								
04H	Mailbox 4	W								
05H	Mailbox 5	W								
06H	Mailbox 6	W								
07H	Mailbox 7	W								
08H	Interrupt_Status	R	1 =	Mailbox* Full	Mailbox** Empty	**MIA RTS***				
			0 =							
09H	Interrupt Mask	R/W	1 =	Enable Full Int	Enable Empty Int	**Enable MIA RTS Int**				Int Pulse 160 ns typ
			0 =	Disable Full Int	Disable Empty Int	**Disable MIA RTS Int**				Int Level
0AH	Status	R	1 =	MIA	Decoder	**MIA RTS**	**MIA CTS**			

*Reading Mailbox 7 will clear this interrupt
**Writing to address 0CH clears this interrupt
*** Writing to address 0DH clears this interrupt

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
				Filled Mailbox	Filled Mailbox	is high	is high			
			0 =	Decoder Read Mailbox	MIA Read Mailbox	MIA RTS is low	MIA CTS is low			
		W	1 =				MIA CTS is high			
			0 =				MIA CTS is low			

0BH	CLK_OUT	R/W		CLK_ENA						Select 1
	6 MHz			1						0
	12 MHz			1						0
	24 MHz			1						1
	off			1						1
	off			0						X
OCH	Clear Mailbox INT	W		Writing to this register clears the mailbox empty interrupt						
ODH	Clear RTS INT	W		Writing to this register clears the MIA RTS interrupt						
OEH	Decode PWR Over ride	R/W		DEC INH PWR_OFF						
			1 =	PWR_ON	X	X	X	X	X	X

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
			0 =	MIA Control						
OFH	PWR STATES	R		DECODER PWR_ON	MIA PWR_ON					
			1 =	ON	ON	X	X	X	X	X
			0 =	OFF	OFF					
			Default	OFF	ON					

Decoder Download (FWE = 1)

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
00H thru 7FH	FLASH ADDR	R/W			Flash Addr bit 6	Flash Addr Bit 5	Flash Addr bit 4	Flash Addr bit 3	Flash Addr bit 2	Flash Addr bit 1
80H	Flash Page	R/W		Flash Addr bit 14	Flash Addr bit 13	Flash Addr bit 12	Flash Addr bit 11	Flash Addr bit 10	Flash Addr bit 9	Flash Addr bit 8
81H	Flash Status	R	1 =	Access Error						0
			0 =	No Error						0
82H	Flash Error	R	1 =	Successful Flash CMD						Unsuccess-ful Erase

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
			0 =	Unsuccess-ful Flash CMD						Successful Erase
83H	**Flash Erase mode**	R/W								**M1**
	Invalid mode									0
	Sector Erase 128B									0
	Page Erase 2KB									1
	Block Erase 32KB									1
84H	**Flash Erase**	W	1 =	**Trim Area Access**	**Reset Flash**	**Pumper off**	Erase bit 4	Erase bit 3	Erase bit 2	Erase bit 1
			0 =	**Flash Area**						

Must write 15H to bit (4:0) to enable a Erase command to the Flash
Must write 00H to bits (4:0) to re-initialize this register before writing another 15H

MIA CPU memory map

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
0000H to 8009H	**CPU Flash**	R								
9000H to 93FFH	**CPU RAM**	R/W								
9400H	**Mailbox0**	R								
9401H	**Mailbox1**	R								
9402H	**Mailbox2**	R								
9403H	**Mailbox3**	R								
9404H	**Mailbox4**	R								
9405H	**Mailbox5**	R								
9406H	**Mailbox6**	R								
9407H	**Mailbox7**	R								

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9400H	Mailbox0	W								
9401H	Mailbox1	W								
9402H	Mailbox2	W								
9403H	Mailbox3	W								
9404H	Mailbox4	W								
9405H	Mailbox5	W								
9406H	Mailbox6	W								
9407H	Mailbox7	W								
9408H	Mailbox status	R	1 =	MIA Filled Mailbox	Decoder Filled Mailbox	**MIA RTS is high**	**MIA CTS is high**			
			0 =	Decoder Read Mailbox	MIA Read Mailbox	**MIA RTS is low**	**MIA CTS is low**			
		W	**1 =**			**MIA RTS is high**				
			0 =			**MIA RTS is low**				
9409H	**Mailbox Interrupt mask**	R/W	1 =	Enable Full Int	Enable Empty Int					
			0 =	Disable Full Int	Disable Empty Int					
940AH	**Mailbox Interrupt**	R	1 =	Mailbox* Full	Mailbox** Empty					

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
			*Reading Mailbox 7 will clear this interrupt							
			**Writing to address 941CH clears this interrupt							
940Bh	Interface Select	R/W		CP_ON	USB_CONN	LED_ON	RES_IN		SE3	SE2
			1 =	on	in	on	on		0	0
			0 =	off	out	off	off		0	0
									0	1
									0	1
									1	0
									1	0
									1	1
									1	1
940CH	Watch Dog control/ status	R/W		WDT	OVR	INT		Run/Stop	S2	S1
			1 =	Generate Reset	Overflow* (read only)	Interupt Enable		Run	0	0
									0	0
									0	1
			0 =	Generate Interrupt	no Overflow	Interrupt Disable		Stop	0	1
									1	0
									1	0
									1	1
									1	1
				* Reading this register will clear the OVR bit if set.						
				** Reading this register will clear the WDT interrupt if set.						
940DH	Watch Dog timer	W		C7	C6	C5	C4	C3	C2	C1
				This is the value to count up from. Rollover causes the Interrupt or Reset						
				Writing this register re-initizes the watchdog counter						
				Watchdog timer is held in reset during Flash write						

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
940EH	**Wake-up control**	R/W		**USB**	**RS485**	**OCIA**	**EXT WAKEUP_IN**	**SYN_CLK**		**CTS**
			1 =	Enable on DIP falling	Enable on Clock_in rising edge	Enable on Clock_out rising edge	Enable on falling edge	Enable on SYN_CLK rising Edge		Enable on CTS falling edge
			0 =	Disable		Disable	Disable	Disable		Disable
940FH	**Wake-up status**	R/W	1 =	USB wakeup	RS485 Wakeup	OCIA Wakeup	EXT Wakeup_in	Synapse Wakeup		CTS Wakeup
				To clear wakeup interrupt, write a '1' to the bits that are set in the Status register.						
9410H	**OCIA control**	R/W		**CLKIN POLARITY**	**CLKOUT POLARITY**	**Data Rcv'ed Interrupt**	**Data Xmitted Interrupt**		**Short/Ext**	**RX_ENA**
			1 =	Clk on rising edge	Clk on rising edge	Interrupt Enable	Interrupt Enable		8 bits	Enable
			0 =	Clk on falling edge	Clk on falling edge	Disable	Disable		9 bits	Disable
9411H	**OCIA status**	R		**Interrupt Flag**						**DR**
			1 =	Interrupt Generated						Data rcv'ed
				Interrupt is cleared when this register is read. DR bit is cleared when rcv data1 or data2 is read. TB bit is cleared when data is loaded into buffer.						

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9412H	OCIA xmit data1	R/W		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9413H	OCIA xmit data2 Ext mode only	R/W								
				To transmit, set bit 0 in the control register to '1'. Then load data in xmit register 2 (Ext only) then xn						
9414H	OCIA rcv data1	R		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9415H	OCIA rcv data2 Ext mode only	R								
9416H	DMA cnt1	R/W		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9417H	DMA cnt2	R/W								bit 9
9418H	DMA addr1 (FIFO address)	R/W						bit 3	bit 2	bit 1
9419H	DMA control	R/W						INT_EN	DMA DIR	
			1 =					Enable Interrupt	Write to RAM	
			0 =					Disable	Read from RAM	

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
				DMA Enable is cleared automatically when the transfer ends.						
941AH	CPU Interrupt Status	R/W		MIA CTS INT *	Wakeup INT	SOF_INT**	WDT_INT	USB_INT	OCIA_INT	Mailbox INT
				*Writing to address 941DH clears this interrupt. **Writing to address 941EH clears this interrupt. ***Writing to address 941FH clears this interrupt. To clear other interrupts, must clear at source.						
941Bh	CPU interrupt mask	R/W		MIA CTS INT_EN		SOF INT_EN				
		1=		Interrupt Enable		Interrupt Enable				
		0 =		Disable		Disable				
941CH	Clear Mailbox INT	W		A write to this register clears the mailbox empty interrupt						
941DH	Clear CTS INT	W		A write to this register clears the MIA CTS interrupt						
941EH	Clear SOF INT	W		A write to this register clears the SOF interrupt						
941FH	Clear DMA INT	W		A write to this register clears the DMA interrupt						
9420H	PWR STATES	R/W		DECODER	MIA					

Address	Register		bit level	bit 7 PWR_ON	bit 6 PWR_ON	bit 5	bit 4	bit 3	bit 2	bit 1
			1 =	ON	ON	X	X	X	X	X
			0 =	OFF	OFF					
			Default	OFF	ON					
9421H	**Decode PWR Over ride**	**R**		**DEC INH PWR_OFF**						
			1 =	PWR_ON	X	X	X	X	X	X
			0 =	MIA Control						
9800H to 982FH	**USB registers**									

bit 0

Int
Active high

Int
Active low

bit 0

Select 0

0
1
0
1
X

X

bit 0

X

bit 0

Flash Addr
bit 0

Flash Addr
bit 7

FLASH
READY

Not Ready

Unsuccess-
ful Write

bit 0

Successful

Write

M0

0

1

0

1

Erase bit 0

bit 0

bit 0

bit 0

SE1

0 OCIA
1 RS232
0 KBD Wedge open
1 KBD Wedge close
0 Synapse
1 IBM Send
0 IBM Receive
1 Wand Emulation

S0

	Resolution
0	3.3 us
1	13.2 us
0	52.8 us
1	211.2 us
0	1.69 ms
1	13.5 ms
0	54.1 ms
1	216.2 ms

C0

bit 0

RXD

Enable on
RXD falling
edge

Disable

RXD
Wakeup

TX_ENA

Enable

Disable

TB empty
Data xmitted

bit 0

bit 0

bit 8

nit register 1.

bit 0 Inverted SDATA

bit 8

bit 0

bit 8

bit 0

DMA_EN

Enable

bit 0

DMA_INT***

bit 0

X

X

EXHIBIT T

mmap_mia

Decoder memory map

Address	Register			bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00H	Mailbox 0		R									
01H	Mailbox 1		R									
02H	Mailbox 2		R									
03H	Mailbox 3		R									
04H	Mailbox 4		R									
05H	Mailbox 5		R									
06H	Mailbox 6		R									
07H	Mailbox 7		R									
00H	Mailbox 0		W									
01H	Mailbox 1		W									
02H	Mailbox 2		W									
03H	Mailbox 3		W									
04H	Mailbox 4		W									
05H	Mailbox 5		W									
06H	Mailbox 6		W									
07H	Mailbox 7		W									
08H	Interrupt_Status		R	1 = Full	Mailbox*		Mailbox**		MIA			RTS***
09H	Interrupt Mask Int Pulse 160 ns typ	R/W Int Active high		1 = Full Int	Enable Int		Enable Empty Int		Enable MIA RTS Int			

*Reading Mailbox 7 will clear this interrupt

**Writing to address OCH clears this interrupt

*** Writing to address ODH clears this interrupt

mmap_mia

			0 =	Disable Full Int	Disable Empty Int	Disable MIA RTS Int	
Int Level		Int Active low					
0AH	Status	R	1 =	MIA Filled Mailbox	Decoder Filled Mailbox	MIA RTS is high	MIA CTS is high
			0 =	Decoder Read Mailbox	MIA Read Mailbox	MIA RTS is low	MIA CTS is low
		W	1 =				MIA CTS is high
			0 =				MIA CTS is low

0BH	CLK_OUT	R/W	CLK_ENA
Select 1	Select 0		
	6 MHz		1
0	0		
	12 MHz		1
0	1		
	24 MHz		1
1	0		
	off		1
1	1		
	off		0
X		X	

OCH	Clear Mailbox INT	W	Writing to this register clears the mailbox empty interrupt

mmap_mia

ODH	Clear RTS INT	W	Writing to this register clears the MIA RTS interrupt

OEH	Decode PWR Over ride	R/W		DEC INH PWR_OFF						
		1 =	PWR_ON	X	X	X	X	X	X	X
		0 =	MIA Control							

OFH	PWR STATES	R		DECODER PWR_ON	MIA PWR_ON					
		1 =	ON	ON	X	X	X	X	X	X
		0 =	OFF	OFF						
		Default	OFF	ON						

Decoder Download (FWE = 1)

Address Register			bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00H thru 7FH	FLASH ADDR	R/W		Flash Addr	Flash Addr	Flash Addr	Flash Addr	Flash Addr	Flash Addr	Flash Addr	Flash Addr
			bit 6	Bit 5	bit 4	bit 3	bit 2	bit 1	bit 0		

80H	Flash Page	R/W		Flash Addr	Flash Addr	Flash Addr	Flash Addr	Flash Addr	Flash Addr
			bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
	bit 7								
81H	Flash Status	R	1 =	Access Error					
0	FLASH READY								
			0 =	No Error					
0	Not Ready								
82H	Flash Error	R	1 =	Successful Flash CMD					
	Unsuccess-ful Erase	Unsuccess-ful Write							
			0 =	Unsuccess-ful Flash CMD					
	Successful Erase	Successful Write							
83H	Flash Erase mode		R/W						
	M1	M0							
0	Invalid mode 0								

Sector Erase 128B
0 1

Page Erase 2KB
1 0

Block Erase 32KB
1 1

84H Flash Erase W Must write 55H to this register to enable a Erase command to the Flash

Must write 00H to re-initialize this register before writing another 55H

MIA CPU memory map

Address	Register	bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0000H to 8009H	CPU Flash	R								
9000H to 93FFH	CPU RAM	R/W								
9400H	Mailbox0	R								
9401H	Mailbox1	R								

9402H	Mailbox2	R						
9403H	Mailbox3	R						
9404H	Mailbox4	R						
9405H	Mailbox5	R						
9406H	Mailbox6	R						
9407H	Mailbox7	R						
9400H	Mailbox0	W						
9401H	Mailbox1	W						
9402H	Mailbox2	W						
9403H	Mailbox3	W						
9404H	Mailbox4	W						
9405H	Mailbox5	W						
9406H	Mailbox6	W						
9407H	Mailbox7	W						
9408H	Mailbox status	R	1 = Filled Mailbox	MIA Filled Mailbox	Decoder MIA RTS is high		MIA CTS	

				mmap_mia			
			0 =	Decoder MIA		MIA RTS	MIA CTS
				Read	Read	is low	is low
				Mailbox	Mailbox		
		W	1 =			MIA RTS	
						is high	
			0 =			MIA RTS	
						is low	
9409H	Mailbox Interrupt		R/W	1 =		Enable	Enable
	mask			Full Int			Empty Int
			0 =	Disable	Disable		
				Full Int			Empty Int
940AH	Mailbox Interrupt		R	1 =		Mailbox*	Mailbox**
				Full	Empty		

*Reading Mailbox 7 will clear this interrupt

**Writing to address 941CH clears this interrupt

940Bh	Interface Select		R/W		CP_ON	USB_CONN	LED_ON	
RES_IN	SE3	SE2	SE1					
		1 =	on	in	on	on	0	0
0	OCIA							
		0 =	off	out	off	off	0	0
1	RS232							
							0	1
0	KBD Wedge open							

1	KBD Wedge close	0	1
0	Synapse	1	0
1	IBM Send	1	0
0	IBM Receive	1	1
1	Wand Emulation	1	1

940CH Watch Dog control/ R/W WDT OVR INT
Run/Stop S2 S1 S0
status
Resolution

			1 =	Generate	Overflow*	Interupt
Run	0	0	0	3.3 us Interrupt	(read only)	Enable
0	0	1	13.2 us			0 1
0	52.8 us		0 =	Generate	no Overflow	Interrupt
Stop	0	1	1	211.2 us reset	Disable	1 0
0	1.69 ms					1 0
1	13.5 ms					1 1
0	54.1 ms					1 1
1	216.2 ms					

* Reading this register will clear the OVR bit if set.

** Reading this register will clear the WDT interrupt if set.

940DH Watch Dog timer W C7 C6 C5 C4 C3 C2 C1 C0

This is the value to count up from. Rollover causes the Interrupt or Reset

Writing this register re-initizes the watchdog counter

Watchdog timer is held in reset during Flash write

940EH Wake-up control R/W USB RS485 OCIA EXT SYN_CLK CTS RXD
WAKEUP_IN

		1 =	Enable on	Enable on	Enable on		
Enable on	Enable on		Enable on	Enable on			
			DIP falling	Clock_in	Clock_out		

					mmap_mia				
falling edge		SYN_CLK		CTS falling		RXD falling			
					rising edge		rising edge		
rising Edge			edge	edge					
			0 =	Disable		Disable	Disable	Disable	
Disable	Disable								

940FH	Wake-up status		R/W	1 =	USB wakeup		RS485	OCIA	EXT
Synapse		CTS	RXD						
					Wakeup	Wakeup	Wakeup_in		Wakeup
Wakeup	Wakeup								

"To clear wakeup interrupt, write a '1' to the bits that are set in the Status register."

9410H	OCIA control		R/W		CLKIN	CLKOUT	Data Rcv'ed		Data Xmitted
	Short/Ext		RX_ENA	TX_ENA					
				POLARITY		POLARITY		Interrupt	
Interrupt									
			1 =	Clk on rising		Clk on rising		Interrupt	
Interrupt			8 bits	Enable	Enable				
				edge	edge	Enable	Enable		
			0 =	Clk on falling		Clk on falling		Disable	Disable
9 bits	Disable	Disable							
				edge	edge				

9411H	OCIA status		R			Interrupt Flag			
	DR	TB empty							
			1 =	Interrupt					
Data rcv'ed		Data xmitted							
				Generated					

Interrupt is cleared when this register is read.

DR bit is cleared when rcv data1 or data2 is read.

TB bit is cleared when data is loaded into buffer.

9412H OCIA xmit data1 R/W bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

9413H OCIA xmit data2 R/W
bit 8
Ext mode only

"To transmit, set bit 0 in the control register to '1'. Then load data in xmit register 2 (Ext only) then xmit register 1."

9414H OCIA rcv data1 R bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0 Inverted SDATA

9415H OCIA rcv data2 R
bit 8
Ext mode only

9416H DMA cnt1 R/W bit 7 bit 6 bit 5 bit 4 bit 3 bit 2 bit 1 bit 0

9417H DMA cnt2 R/W
bit 9 bit 8

9418H DMA addr1 R/W bit 3 bit 2 bit 1 bit 0
(FIFO address)

9419H DMA control R/W INT_EN DMA DIR DMA_EN

1 = Enable Write to

mmap_mia

Enable

Interrupt RAM

0 = Disable Read from

RAM

DMA Enable is cleared automatically when the transfer ends.

941AH CPU interrupt R/W MIA CTS Wakeup SOF_INT** WDT_INT USB_INT OCIA_INT Mailbox DMA_INT***
Status INT * INT INT

*Writing to address 941DH clears this interrupt.

**Writing to address 941EH clears this interrupt.

***Writing to address 941FH clears this interrupt.

"To clear other interrupts, must clear at source."

941Bh CPU interrupt R/W MIA CTS SOF INT_EN
mask INT_EN

1= Interrupt Interrupt
Enable Enable

0 = Disable Disable

941CH Clear Mailbox INT W A write to this register clears the mailbox empty interrupt

mmap_mia

941DH Clear CTS INT W A write to this register clears the MIA CTS interrupt

941EH Clear SOF INT W A write to this register clears the SOF interrupt

941FH Clear DMA INT W A write to this register clears the DMA interrupt

9420H PWR STATES R/W DECODER MIA

	PWR_ON	PWR_ON						
1 =	ON	ON	X	X	X	X	X	X
0 =	OFF	OFF						
Default	OFF	ON						

9421H Decode PWR Over ride R DEC INH PWR_OFF

	PWR_ON	X	X	X	X	X	X	X
1 =	PWR_ON	X	X	X	X	X	X	X
0 =	MIA Control							

9800H to 982FH USB registers

EXHIBIT U

Decoder memory map

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
00H	Mailbox 0	R								
01H	Mailbox 1	R								
02H	Mailbox 2	R								
03H	Mailbox 3	R								
04H	Mailbox 4	R								
05H	Mailbox 5	R								
06H	Mailbox 6	R								
07H	Mailbox 7	R								
00H	Mailbox 0	W								
01H	Mailbox 1	W								
02H	Mailbox 2	W								
03H	Mailbox 3	W								
04H	Mailbox 4	W								
05H	Mailbox 5	W								
06H	Mailbox 6	W								
07H	Mailbox 7	W								
08H	Interrupt_Status	R	1 =	Mailbox* Full	Mailbox** Empty	**MIA RTS***				
09H	Interrupt Mask	R/W	1 =	Enable Full Int	Enable Empty Int	**Enable MIA RTS Int**				Int Pulse 160 ns typ
			0 =	Disable Full Int	Disable Empty Int	**Disable MIA RTS Int**				Int Level
0AH	Status	R	1 =	MIA	Decoder	**MIA RTS**	**MIA CTS**			

*Reading Mailbox 7 will clear this interrupt
**Writing to address 0CH clears this interrupt
*** Writing to address 0DH clears this interrupt

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
				Filled Mailbox	Filled Mailbox	is high	is high			
			0 =	Decoder Read Mailbox	MIA Read Mailbox	MIA RTS is low	MIA CTS is low			
		W	1 =				MIA CTS is high			
			0 =				MIA CTS is low			
0BH	CLK_OUT	R/W		CLK_ENA						Select 1
	6 MHz			1						0
	12 MHz			1						0
	24 MHz			1						1
	off			1						1
	off			0						X
OCH	Clear Mailbox INT	W		Writing to this register clears the mailbox empty interrupt						
ODH	Clear RTS INT	W		Writing to this register clears the MIA RTS interrupt						
OEH	Decode PWR Over ride	R/W		DEC INH PWR_OFF						
			1 =	PWR_ON	X	X	X	X	X	X

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
			0 =	MIA Control						
				* Wrire only, self clearing						
OFH	PWR STATES	R		DECODER PWR_ON	MIA PWR_ON					
			1 =	ON	ON	X	X	X	X	X
			0 =	OFF	OFF					
			Default	OFF	ON					
10H	Version Register	R		0	0	0	0	0	0	0

Decoder Download (FWE = 1)

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
00H thru 7FH	FLASH ADDR	R/W			Flash Addr bit 6	Flash Addr Bit 5	Flash Addr bit 4	Flash Addr bit 3	Flash Addr bit 2	Flash Addr bit 1
80H	Flash Page	R/W		Flash Addr bit 14	Flash Addr bit 13	Flash Addr bit 12	Flash Addr bit 11	Flash Addr bit 10	Flash Addr bit 9	Flash Addr bit 8
81H	Flash Status	R	1 =	Access Error						0
			0 =	No Error						0
82H	Flash Error	R	1 =	Successful Flash CMD					Successful extended	Unsuccess-ful Erase

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
									erase	
			0 =	Unsuccess-ful Flash CMD					Unsuccess-ful extended erase	Successful Erase
83H	**Flash Erase mode** Invalid mode Sector Erase 128B Page Erase 2KB Block Erase 32KB	R/W							**Sector Protect**	**M1** 0 0 1 1
84H	**Flash Erase**	W	1 =	**Trim Area Access**	**Pumper off**	**Flash_rst**	Erase bit 4	Erase bit 3	Erase bit 2	Erase bit 1
			0 =	**Flash Area**						

Must write 15H to bit (4:0) to enable a Erase command to the Flash
Must write 00H to bits (4:0) to re-initialize this register before writing another 15H

EBH	**ESWCNT**	R/W	Soft write pulse counter in SFR space, Trim Area = '1'
ECH	**ERCNT1**	R/W	Erase pulse counter register adaptive erase in SFR space, Trim Area = '1'
EDH	**ERCNT0**	R/W	Erase pulse counter register initial erase in SFR space, Trim Area = '1
EEH	**ECNTV4**	R/W	Write pulse count register for less than 5V in SFR space, Trim Area = '1'
EFH	**ECNTV5**	R/W	Write pulse count register for 5V in SFR space, Trim Area = '1
F3H	**ERPCNT**	**R**	Erase pulse count in SFR space, Trim Area = '1'

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
F4H	ERADDRL	R/W		LSByte of Erase-Error Address in SFR space, Time Area = '1'						
F5H	ERADDRH	R/W		MSByte of Erase-Error Address in SFR space, Trim Area = '1'						
F6H	EWADDRL	R		LSByte of Erase-Wrire error Address in SFR space, Trim Area = '1'						
F7H	EWADDRH	R		MSByte of Erase-Wrire error Address in SFR space, Trim Area = '1'						
FBH	RDPULSES	R/W		Read Pulse count register in SFR space, Trim Area = '1'						
FCH	FMDC	R/W		EPsen	HIsen_f	MIsen_f	HVGsen_f	ppmp_to	HIsen	MIsen
FDH	FMEDC	R/W		aprg_dis	SoftPrgen	EDAC1	EDAC0	BGmsb	Aprg_cnt2	Aprg_cnt1
FEH	BGTRIM	R/W		Band Gap Reference Trim bits in SFR space, Trim Area = '1'						
FFH	APC	R/W		Adaptive pulse count in SFR space, Trim Area = '1'						

MIA CPU memory map

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
0000H to 8009H	CPU Flash	R								
9000H to 93FFH	CPU RAM	R/W								
9400H	Mailbox0	R								
9401H	Mailbox1	R								
9402H	Mailbox2	R								
9403H	Mailbox3	R								
9404H	Mailbox4	R								
9405H	Mailbox5	R								
9406H	Mailbox6	R								
9407H	Mailbox7	R								

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9400H	Mailbox0	W								
9401H	Mailbox1	W								
9402H	Mailbox2	W								
9403H	Mailbox3	W								
9404H	Mailbox4	W								
9405H	Mailbox5	W								
9406H	Mailbox6	W								
9407H	Mailbox7	W								
9408H	Mailbox status	R	1 =	MIA Filled Mailbox	Decoder Filled Mailbox	**MIA RTS is high**	**MIA CTS is high**			
			0 =	Decoder Read Mailbox	MIA Read Mailbox	**MIA RTS is low**	**MIA CTS is low**			
		W	1 =			**MIA RTS is high**				
			0 =			**MIA RTS is low**				
9409H	Mailbox Interrupt mask	R/W	1 =	Enable Full Int	Enable Empty Int					
			0 =	Disable Full Int	Disable Empty Int					
940AH	Mailbox Interrupt	R	1 =	Mailbox* Full	Mailbox** Empty					

*Reading Mailbox 7 will clear this interrupt

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	
			**Writing to address 941CH clears this interrupt								
940Bh	Interface Select	R/W		CP_ON	USB_CONN	SDCI_EN	RES_IN	CABLE_DET	SE3	SE2	
			1 =	on	in	on	on	on	0	0	
			0 =	off	out	off	off	off	0	0	
									0	1	
									0	1	
									1	0	
									1	0	
									1	1	
									1	1	
940CH	Watch Dog control/ status	R/W		WDT	OVR	INT		Run/Stop	S2	S1	
			1 =	Generate Reset	Overflow* (read only)	Interupt Enable		Run	0	0	
									0	0	
									0	1	
			0 =	Generate Interrupt	no Overflow	Interrupt Disable		Stop	0	1	
									1	0	
									1	0	
									1	1	
									1	1	
				* Reading this register will clear the OVR bit if set.							
				** Reading this register will clear the WDT interrupt if set.							
940DH	Watch Dog timer	W		C7	C6	C5	C4	C3	C2	C1	
				This is the value to count up from. Rollover causes the Interrupt or Reset							
				Writing this register re-initizes the watchdog counter							
				Watchdog timer is held in reset during Flash write							

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
940EH	Wake-up control	R/W		USB	RS485	OCIA	EXT WAKEUP_IN	SYN_CLK		CTS
			1 =	Enable on DIP falling	Enable on Clock_in rising edge	Enable on Clock_out rising edge	Enable on falling edge	Enable on SYN_CLK rising Edge		Enable on CTS falling edge
			0 =	Disable		Disable	Disable	Disable		Disable
940FH	Wake-up status	R/W	1 =	USB wakeup	RS485 Wakeup	OCIA Wakeup	EXT Wakeup_in	Synapse Wakeup		CTS Wakeup
				To clear wakeup interrupt, write a '1' to the bits that are set in the Status register.						
9410H	OCIA control	R/W		CLKIN POLARITY	CLKOUT POLARITY	Data Rcv'ed Interrupt	Data Xmitted Interrupt		Short/Ext	RX_ENA
			1 =	Clk on rising edge	Clk on rising edge	Interrupt Enable	Interrupt Enable		8 bits	Enable
			0 =	Clk on falling edge	Clk on falling edge	Disable	Disable		9 bits	Disable
9411H	OCIA status	R		Interrupt Flag						DR
			1 =	Interrupt Generated						Data rcv'ed
				Interrupt is cleared when this register is read. DR bit is cleared when rcv data1 or data2 is read. TB bit is cleared when data is loaded into buffer.						

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9412H	**OCIA xmit data1**	R/W		bit 7	bit 6	bit 5	blt 4	bit 3	bit 2	bit 1
9413H	**OCIA xmit data2** Ext mode only	R/W								
				To transmit, set bit 0 in the control register to '1'. Then load data in xmit register 2 (Ext only) then xn						
9414H	**OCIA rcv data1**	R		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9415H	**OCIA rcv data2** Ext mode only	R								
9416H	**DMA cnt1**	R/W		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
9417H	**DMA cnt2**	R/W								bit 9
9418H	**DMA addr1** (FIFO address)	R/W						bit 3	bit 2	bit 1
9419H	**DMA control**	R/W						**INT_EN**	**DMA DIR**	
			1 =					Enable Interrupt	Write to RAM	
			0 =					Disable	Read from RAM	
				DMA Enable is cleared automatically when the transfer ends.						

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
941AH	CPU interrupt Status	R/W		MIA CTS INT *	Wakeup INT	SOF_INT**	WDT_INT	USB_INT	OCIA_INT	Mailbox INT
				*Writing to address 941DH clears this interrupt. **Writing to address 941EH clears this interrupt. ***Writing to address 941FH clears this interrupt. To clear other interrupts, must clear at source.						
941BH	CPU interrupt mask	R/W		MIA CTS INT_EN		SOF INT_EN				
		1=		Interrupt Enable		Interrupt Enable				
		0 =		Disable		Disable				
941CH	Clear Mailbox INT	W		A write to this register clears the mailbox empty interrupt						
941DH	Clear CTS INT	W		A write to this register clears the MIA CTS interrupt						
941EH	Clear SOF INT	W		A write to this register clears the SOF interrupt						
941FH	Clear DMA INT	W		A write to this register clears the DMA interrupt						
9420H	PWR STATES	R/W		DECODER PWR_ON	MIA PWR_ON					

Address	Register		bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
			1 =	ON	ON	X	X	X	X	X
			0 =	OFF	OFF					
			Default	OFF	ON					
9421H	**Decode PWR Over ride**	R		**DEC INH PWR_OFF**						
			1 =	PWR_ON	X	X	X	X	X	X
			0 =	MIA Control						
9422H	**CPU interrupt Status2**	R								
				*Writing to address 9424H clears this interrupt.						
9423H	**CPU interrupt mask2**	R/W								
		1=								
		0 =								
9424H	**Clear RS232 CTS INT**	W		**A write to this register clears the RS232 CTS interrupt**						
9425H	**Version Register**	R		0	0	0	0	0	0	0

Address	Register	bit level	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1
A000H to A3FFH	Test USB RAM								

bit 0

Int
Active high

Int
Active low

bit 0

Select 0

0
1
0
1
X

SOFT_RESET*

Reset ASIC

bit 0

X

1

bit 0

Flash Addr
bit 0

Flash Addr
bit 7

FLASH
READY

Not Ready

Unsuccess-
ful Write

bit 0

Successful
Write

M0

0
1
0
1

Erase bit 0

bit 0

HVGsen

Aprg_cnt0

bit 0

bit 0

bit 0

SE1

0 OCIA
1 RS232
0 KBD Wedge open
1 KBD Wedge close
0 Synapse
1 IBM Send
0 IBM Receive
1 Wand Emulation

S0

	Resolution
0	3.3 us
1	13.2 us
0	52.8 us
1	211.2 us
0	1.69 ms
1	13.5 ms
0	54.1 ms
1	216.2 ms

C0

bit 0

RXD

Enable on
RXD falling
edge

Disable

RXD
Wakeup

TX_ENA

Enable

Disable

TB empty
Data xmitted

bit 0

DMA_INT***

bit 0

X

X

RS232 CTS INT*

RS232 CTS INT_EN

Interrupt Enable

Disable

bit 0

EXHIBIT V

Comparision between Alcatel's and UTMC's quote for Multi-Interface ASIC

	Alcatel	UTMC	Remark
NRE cost	$238,000	$200,000	
Unit cost	$2.46	$2.93	500K price for 2001
Technology	0.7um	0.35um	
Package	TQFP64	TQFP52	
Turnkey Design	Yes	No	
Total embedded RAM	1.2KB	2.8KB	
embedded FLASH	None	32KB	The key factor
USB Core	Yes	Yes	
Microprocessor core	No	Yes	Alcatel has a core but i
RS232 with +/-5V swing	Yes	Yes	Reason why these two
Risk	Low	Higher	
Lead Time to protos	6-7mo	9-10mo	
Own Foundry	Yes	No	

Note:
1. The UTMC's triple-well technologies is new and UTMC is fabless
the proposed foundry is Hyundai.
2. The lead time is time to get the first prototype
and the estimated UTMC lead time has added a 3-4 month
of Symbol development time.

it is not included in this price
vendors are only in consideration

EXHIBIT W

Mechanics of Handshake between MIA and Decoder

The MIA will generate a RTS to the Decoder.

The Decoder will generate a CTS to the MIA.

RTS:

1 – Decoder sets **Interrupt mask register** bit 5 to '1'.
2 – MIA writes a '1' to **CPU Mailbox Status register** bit 5.
3 – The RTS bit in the **Decoder Mailbox Status register** (bit 5) gets set.
4 – An interrupt is generated to the Decoder.
5 – The Decoder reads his **Interrupt Status register** to see that a RTS caused the interrupt.
6 – The Decoder clears the Interrupt (HOW?).

CTS:

7 – The CPU sets his **Interrupt Mask register** bit 7 to '1'.
8 - Decoder writes a '1' to **Decoder Mailbox Status register** bit 4.
9 - The CTS bit in the **CPU Mailbox Status register** (bit 4) gets set.
10 - An interrupt is generated to the CPU.
11 - The CPU reads his **Interrupt Status register** to see that a CTS caused the interrupt.
12 – The CPU clears the Interrupt (HOW?).

RTS:

12 – MIA writes a '0' to **CPU Mailbox Status register** bit 5.
13 – The RTS bit in the **Decoder Mailbox Status register** (bit 5) gets cleared.
14 – An interrupt is generated to the Decoder.
15 – The Decoder reads his **Interrupt Status register** to see that a RTS caused the interrupt.
16 – The Decoder clears the Interrupt (HOW?).

CTS:

17 - Decoder writes a '0' to **Decoder Mailbox Status register** bit 4.
18 - The CTS bit in the **CPU Mailbox Status register** (bit 4) gets cleared.
19 - An interrupt is generated to the CPU.
20 - The CPU reads his **Interrupt Status register** to see that a CTS caused the interrupt.
21 – The CPU clears the Interrupt (HOW?).

EXHIBIT X

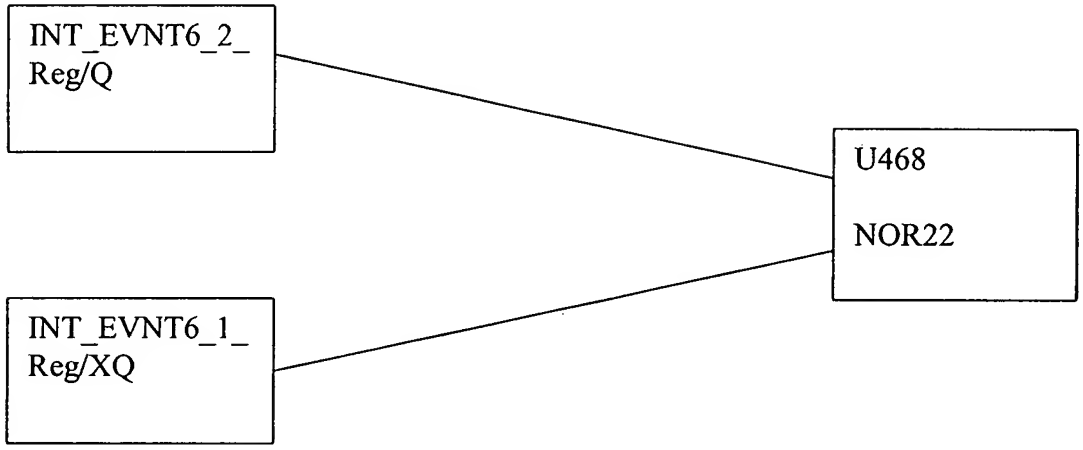
Date						
Firm		Required	Alcatel	UTMC	Hyundai	Epson
Business Issues	Annual division sales dollars					
Business Issues	Annual sales dollars					
Business Issues	Debt to Equity ratio					
Business Issues	Division or Parent					
Business Issues	EPS (latest data available)					
Business Issues	Fab locations		France	Fabless		
Business Issues	Headquarters location		France	Colarado		
Business Issues	Number of Employees					
Business Issues	Public or privately held?		Public	Public		
Business Issues	Rep Firm					
Business Issues	Stock Exchange					
Business Issues	Trading symbol					
Cell Config	Gate Array					
Cell Config	Standard Cell Based		Yes	Yes		
Complexity	Max Metal Layers Avail			3		
Cores or features available	ATPG					
Cores or features available	Customer Owned Tooling (COT)					
Cores or features available	Embedded DRAM					
Cores or features available	Embedded Flash	Yes	No	32KB		
Cores or features available	Embedded Micro	Yes	Yes	Yes		
Cores or features available	Embedded SRAM					
Cores or features available	Industrial Temp	Yes	Yes	Yes		
Cores or features available	IP Cores Available		Yes	Yes		
Cores or features available	JTAG					
Cores or features available	Libraries		Yes	Yes		
Cores or features available	Microprocessor core		No	Yes		Alcatel has a core but it is not included in this price
Cores or features available	PLL		Yes	Yes		
Cores or features available	Total embedded RAM		1.2KB	2.8KB		
Cores or features available	UARTs	Yes	Yes	Yes		
Cores or features available	USB	Yes	Yes	Yes		
Cost	Cost Improvement p/qtr					
Cost	NRE		$238,000.00	$200,000.00		
Cycle time	Consignment					
Cycle time	Design lead-times					
Cycle time	Distribution					
Cycle time	Expedites available?					
Cycle time	Factory Stocking Program					
Cycle time	Production lead-times					
Cycle time	proto lead-times		6-7mo	9-10mo		
Design Support	Altera Conversion Experience					
Design Support	Design Tools					
Design Support	Local Support available in: (City)					
Design Support	Xilinx Conversion Experience					
Other	EOL Policy					
Other	PCN Policy					
Other	RS232 with +/-5V swing	Yes	Yes	Yes		
Other	Turnkey Design		Yes	No		
Other			TQFP64	TQFP52		
Packaging	Bare Die					
Packaging	BGA					
Packaging	Chip Scale Package					
Packaging	Die Bank					
Packaging	Flip Chip					
Packaging	Known Good Die program?					
Packaging	Micro BGA					
Process Technology	.15 Micron					
Process Technology	.18 Micron					
Process Technology	.25 micron					
Process Technology	.30 Micron					
Process Technology	.35 Micron			0.35		
Process Technology	.50 Micron					
Process Technology	.60 Micron					
Process Technology	.65 Micron					
Process Technology	.80 Micron		0.7			
Process Technology	Greater then .80 Micron					
Quailty	ISO9000 Certified					
Quailty	RML Tier					
Signal Type	Analog signal					
Signal Type	Digital signal					
Signal Type	Mixed Signal		Yes	Yes		

Note:
1. The UTMC's triple-well technologies is new and UTMC is fabless the proposed foundry is Hyundai.
2. The lead time is time to get the first prototype and the estimated UTMC lead time has added a 3-4 month of Symbol development time.

EXHIBIT Y

Change for MIA ASIC in Write_reg block

Change from:



To:

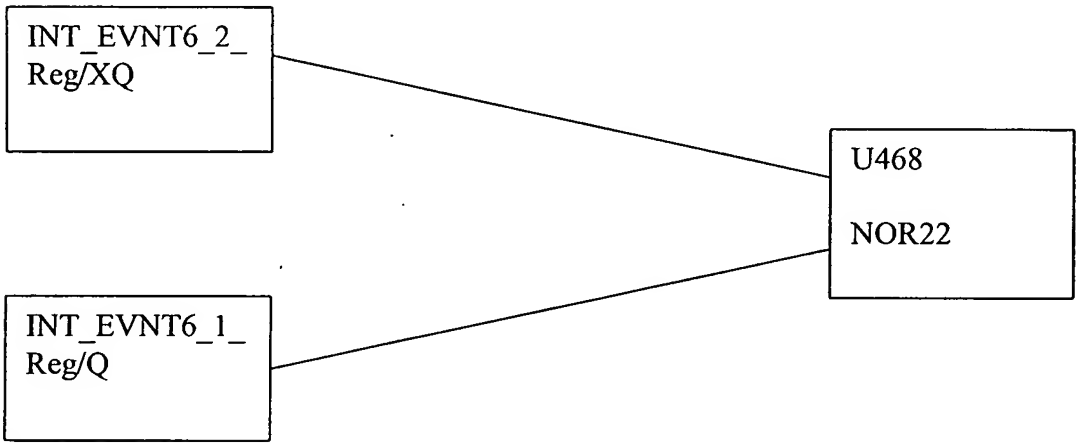


EXHIBIT Z

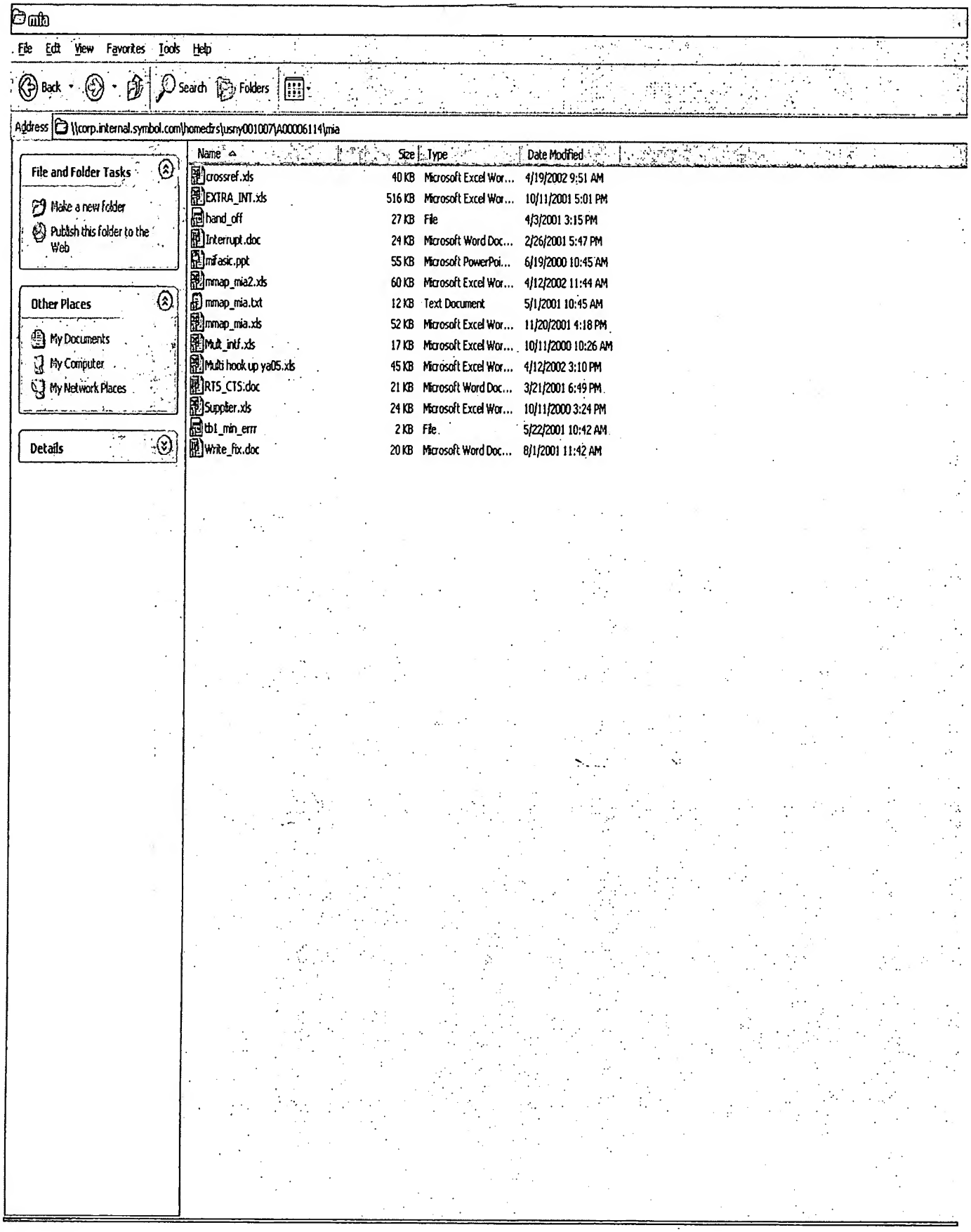

mia
File Edit View Favorites Tools Help
Back Search Folders
Address \\corp.internal.symbol.com\homedirs\usny001007\A00006114\mia
File and Folder Tasks
Make a new folder
Publish this folder to the Web
Other Places
My Documents
My Computer
My Network Places
Details
Name Size Type Date Modified
crossref.xls 40 KB Microsoft Excel Wor... 4/19/2002 9:51 AM
EXTRA_INT.xls 516 KB Microsoft Excel Wor... 10/11/2001 5:01 PM
hand_off 27 KB File 4/3/2001 3:15 PM
Interrupt.doc 24 KB Microsoft Word Doc... 2/26/2001 5:47 PM
miasic.ppt 55 KB Microsoft PowerPoi... 6/19/2000 10:45 AM
mmap_mia2.xls 60 KB Microsoft Excel Wor... 4/12/2002 11:44 AM
mmap_mia.txt 12 KB Text Document 5/1/2001 10:45 AM
mmap_mia.xls 52 KB Microsoft Excel Wor... 11/20/2001 4:18 PM
Mult_intf.xls 17 KB Microsoft Excel Wor... 10/11/2000 10:26 AM
Multi hook up ya05.xls 45 KB Microsoft Excel Wor... 4/12/2002 3:10 PM
RTS_CTS.doc 21 KB Microsoft Word Doc... 3/21/2001 6:49 PM
Supplier.xls 24 KB Microsoft Excel Wor... 10/11/2000 3:24 PM
tb1_min_errr 2 KB File 5/22/2001 10:42 AM
Write_fix.doc 20 KB Microsoft Word Doc... 8/1/2001 11:42 AM

EXHIBIT AA

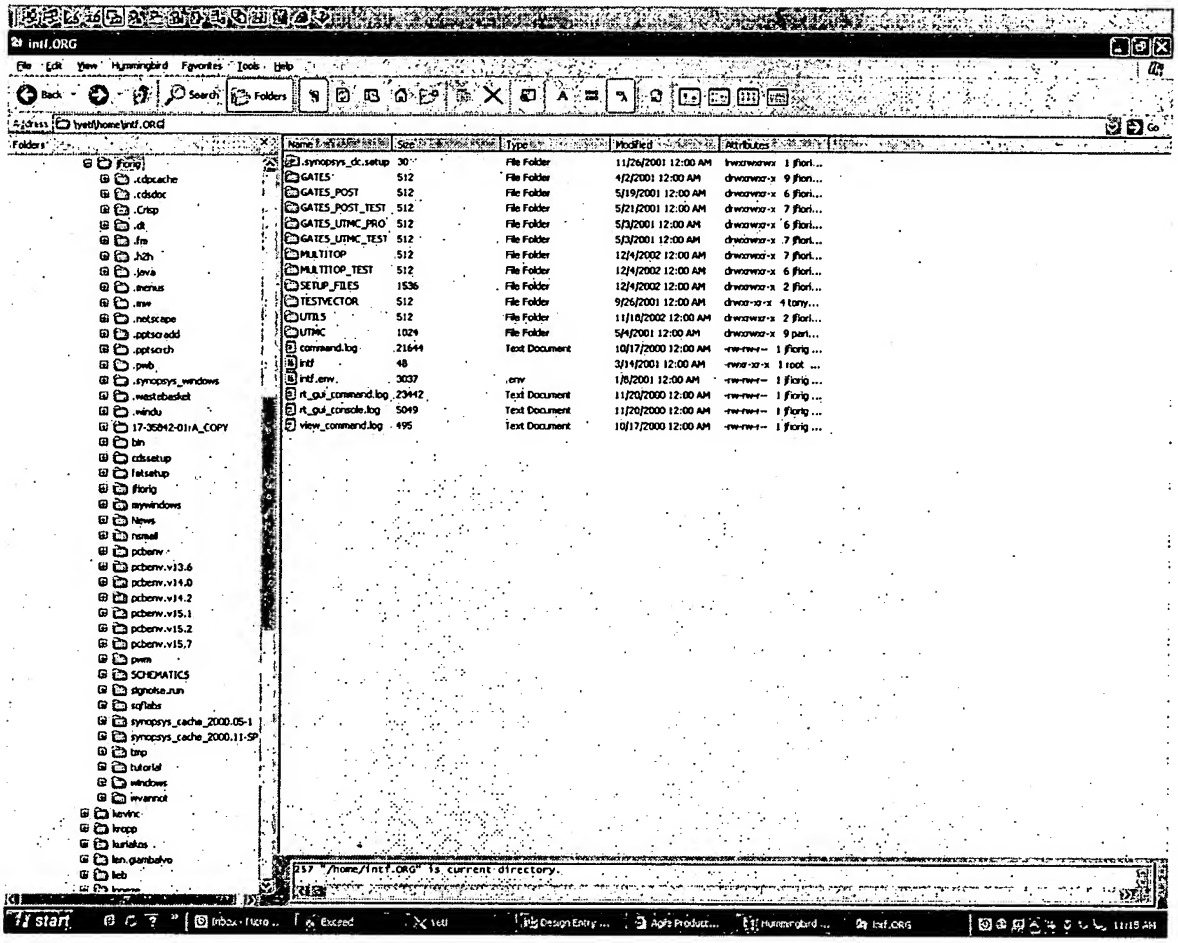

intf.ORG
File Edit View Hummingbird Favorites Tools Help
Back Search Folders
Address tyetf\home\intf.ORG
Folders
jfiorig
.cdscache
.cdsdoc
.Crisp
.dt
.fm
.h2h
.java
.menus
.mw
.netscape
.optscradd
.optscrch
.pwb
.synopsys_windows
.westcbasket
.windu
17-35842-01rA_COPY
bin
cdssetup
fetsetup
jfiorig
mywindows
News
nsmail
pcbenv
pcbenv.v13.6
pcbenv.v14.0
pcbenv.v14.2
pcbenv.v15.1
pcbenv.v15.2
pcbenv.v15.7
pwm
SCHEMATICS
signoise.run
sqllabs
synopsys_cache_2000.05-1
synopsys_cache_2000.11-SP
tmp
tutorial
windows
mvannot
kevinc
knopp
kuriakos
len.gambalvo
leb
Name Size Type Modified Attributes
.synopsys_dc.setup 30 File Folder 11/26/2001 12:00 AM lrwxrwxrwx 1 jfiori...
GATES 512 File Folder 4/2/2001 12:00 AM drwxrwxr-x 9 jfiori...
GATES_POST 512 File Folder 5/19/2001 12:00 AM drwxrwxr-x 6 jfiori...
GATES_POST_TEST 512 File Folder 5/21/2001 12:00 AM drwxrwxr-x 7 jfiori...
GATES_UTMC_PRO 512 File Folder 5/3/2001 12:00 AM drwxrwxr-x 6 jfiori...
GATES_UTMC_TEST 512 File Folder 5/3/2001 12:00 AM drwxrwxr-x 7 jfiori...
MULTITOP 512 File Folder 12/4/2002 12:00 AM drwxrwxr-x 7 jfiori...
MULTITOP_TEST 512 File Folder 12/4/2002 12:00 AM drwxrwxr-x 6 jfiori...
SETUP_FILES 1536 File Folder 12/4/2002 12:00 AM drwxrwxr-x 2 jfiori...
TESTVECTOR 512 File Folder 9/26/2001 12:00 AM drwxr-xr-x 4 tony...
UTILS 512 File Folder 11/18/2002 12:00 AM drwxrwxr-x 2 jfiori...
UTMC 1024 File Folder 5/4/2001 12:00 AM drwxrwxr-x 9 pari...
command.log 21644 Text Document 10/17/2000 12:00 AM -rw-rw-r-- 1 jfiorig ...
intf 48 3/14/2001 12:00 AM -rwxr-xr-x 1 root ...
intf.env. 3037 .env 1/8/2001 12:00 AM -rw-rw-r-- 1 jfiorig ...
rt_gui_command.log 23442 Text Document 11/20/2000 12:00 AM -rw-rw-r-- 1 jfiorig ...
rt_gui_console.log 5049 Text Document 11/20/2000 12:00 AM -rw-rw-r-- 1 jfiorig ...
view_command.log 495 Text Document 10/17/2000 12:00 AM -rw-rw-r-- 1 jfiorig ...
257 "/home/intf.ORG" is current directory.
start
Inbox - Micro...
Excel
Test
Design Entry ...
Agile Product...
Hummingbird ...
intf.ORG
11:15 AM

EXHIBIT BB

Drives from viewpoint of Multiwrap		
Multiwrap Port Name	Net Name at Multiwrap Port	All layer Respin YA05A Port Names
A0	A0_IN	A0
AD_A(0)	AD_A_0_port	AD_A 0
AD_A(1)	AD_A_1_port	AD_A 1
AD_A(2)	AD_A_2_port	AD_A 2
AD_A(3)	AD_A_3_port	AD_A 3
AD_A(4)	AD_A_4_port	AD_A 4
AD_A(5)	AD_A_5_port	AD_A 5
AD_A(6)	AD_A_6_port	AD_A 6
AD_A(7)	AD_A_7_port	AD_A 7
AD_EN	AD_EN_N	AD_EN
ALE	ALE_IN	ALE
B1_IN	B1_IN	B1_IN
B2_IN	B2_IN	B2_IN
B3_IN	B3_IN	B3_IN
BAUD_CLK	BAUD_CLK	BAUD_CLK
BGTRIM 0		BGTRIM 0
BGTRIM 1		BGTRIM 1
BGTRIM 2		BGTRIM 2
BGTRIM 3		BGTRIM 3
BGTRIM 4		BGTRIM 4
BGTRIM 5		BGTRIM 5
BGTRIM 6		BGTRIM 6
BGTRIM 7		BGTRIM 7
bgtrim8		*bgtrim8*
CLK_OUT	DEC_CLKOUT	CLK_OUT
COSC	CPU_OSC	COSC
CPU_ADDR(0)	CPU_ADDR_0_port	CPU_ADDR 0
CPU_ADDR(1)	CPU_ADDR_1_port	CPU_ADDR 1
CPU_ADDR(10)	CPU_ADDR_10_port	CPU_ADDR 10
CPU_ADDR(11)	CPU_ADDR_11_port	CPU_ADDR 11
CPU_ADDR(12)	CPU_ADDR_12_port	CPU_ADDR 12
CPU_ADDR(13)	CPU_ADDR_13_port	CPU_ADDR 13
CPU_ADDR(14)	CPU_ADDR_14_port	CPU_ADDR 14
CPU_ADDR(15)	CPU_ADDR_15_port	CPU_ADDR 15
CPU_ADDR(2)	CPU_ADDR_2_port	CPU_ADDR 2
CPU_ADDR(3)	CPU_ADDR_3_port	CPU_ADDR 3
CPU_ADDR(4)	CPU_ADDR_4_port	CPU_ADDR 4
CPU_ADDR(5)	CPU_ADDR_5_port	CPU_ADDR 5
CPU_ADDR(6)	CPU_ADDR_6_port	CPU_ADDR 6
CPU_ADDR(7)	CPU_ADDR_7_port	CPU_ADDR 7
CPU_ADDR(8)	CPU_ADDR_8_port	CPU_ADDR 8
CPU_ADDR(9)	CPU_ADDR_9_port	CPU_ADDR 9
CPU_PSEN	CPU_PSEN	CPU_PSEN
CPU_RD	CPU_RD	CPU_RD
CPU_WR	CPU_WR	CPU_WR
CP_ON	CP_ON	CP_ON
CS_N	CS	CS
DIDIF	DIDIF	DIDIF
DIM	DIM	DIM
DIP	DIP	DIP
DMA_ACK	DACK	*dma_ack_sdci_clk_in*
DMA_REQ	DMA_REQUEST	DMA_REQ
DOM	DOM	DOM
DOP	DOP	DOP
DOWNLOAD_OUT_N	DOWNLOAD_OUT_N	*now output from Analog*
D_IN(0)	D_IN_0_port	D_IN 0

D_IN(1)	D_IN_1_port	D_IN 1
D_IN(2)	D_IN_2_port	D_IN 2
D_IN(3)	D_IN_3_port	D_IN 3
D_IN(4)	D_IN_4_port	D_IN 4
D_IN(5)	D_IN_5_port	D_IN 5
D_IN(6)	D_IN_6_port	D_IN 6
D_IN(7)	D_IN_7_port	D_IN 7
D_OUT(0)	D_OUT_0_port	D_OUT 0
D_OUT(1)	D_OUT_1_port	D_OUT 1
D_OUT(2)	D_OUT_2_port	D_OUT 2
D_OUT(3)	D_OUT_3_port	D_OUT 3
D_OUT(4)	D_OUT_4_port	D_OUT 4
D_OUT(5)	D_OUT_5_port	D_OUT 5
D_OUT(6)	D_OUT_6_port	D_OUT 6
D_OUT(7)	D_OUT_7_port	D_OUT 7
D_OUT_EN	N_RD	D_OUT_EN
EMULATE_EN_N	EMULATE_EN_N	EMULATE_EN_N
EMU_EN	EMU_EN	EMULATE_EN
EOT	EOT	EOT
EXT_ADDR_IN(10)	EXT_ADDR_IN_10_port	EMU_ADDR_IN 10
EXT_ADDR_IN(11)	EXT_ADDR_IN_11_port	EMU_ADDR_IN 11
EXT_ADDR_IN(12)	EXT_ADDR_IN_12_port	EMU_ADDR_IN 12
EXT_ADDR_IN(13)	EXT_ADDR_IN_13_port	EMU_ADDR_IN 13
EXT_ADDR_IN(14)	EXT_ADDR_IN_14_port	EMU_ADDR_IN 14
EXT_ADDR_IN(15)	EXT_ADDR_IN_15_port	EMU_ADDR_IN 15
EXT_ADDR_IN(8)	EXT_ADDR_IN_8_port	EMU_ADDR_IN 8
EXT_ADDR_IN(9)	EXT_ADDR_IN_9_port	EMU_ADDR_IN 9
EXT_AD_IN(0)	EXT_AD_IN_0_port	EMU_AD_IN 0
EXT_AD_IN(1)	EXT_AD_IN_1_port	EMU_AD_IN 1
EXT_AD_IN(2)	EXT_AD_IN_2_port	EMU_AD_IN 2
EXT_AD_IN(3)	EXT_AD_IN_3_port	EMU_AD_IN 3
EXT_AD_IN(4)	EXT_AD_IN_4_port	EMU_AD_IN 4
EXT_AD_IN(5)	EXT_AD_IN_5_port	EMU_AD_IN 5
EXT_AD_IN(6)	EXT_AD_IN_6_port	EMU_AD_IN 6
EXT_AD_IN(7)	EXT_AD_IN_7_port	EMU_AD_IN 7
EXT_ALE	EXT_ALE	EMU_ALE
EXT_MEM_RD	EXT_MEM_RD	EMU_MEMR
EXT_MEM_WR	EXT_MEM_WR	EMU_MEMW
EXT_PORT1_IN(0)	EXT_P1_IN_0_port	
EXT_PORT1_IN(1)	EXT_P1_IN_1_port	*emu_p11_in*
EXT_PORT1_IN(2)	EXT_P1_IN_2_port	
EXT_PORT1_IN(3)	EXT_P1_IN_3_port	
EXT_PORT1_IN(4)	EXT_P1_IN_4_port	
EXT_PORT1_IN(5)	EXT_P1_IN_5_port	
EXT_PORT1_IN(6)	EXT_P1_IN_6_port	*emu_p16_in*
EXT_PORT1_IN(7)	EXT_P1_IN_7_port	
EXT_PORT3_IN(0)	EXT_P3_IN_0_port	
EXT_PORT3_IN(1)	EXT_P3_IN_1_port	*emu_p31_in*
EXT_PORT3_IN(2)	EXT_P3_IN_2_port	
EXT_PORT3_IN(3)	EXT_P3_IN_3_port	
EXT_PORT3_IN(4)	EXT_P3_IN_4_port	
EXT_PORT3_IN(5)	EXT_P3_IN_5_port	
EXT_PORT3_IN(6)	EXT_P3_IN_6_port	
EXT_PORT3_IN(7)	EXT_P3_IN_7_port	
EXT_PSEN	EXT_PSEN	EMU_PSEN
EXT_WAKEUP	EXT_WAKEUP	EXT_WAKEUP
EXT_WDT_INH	EXT_WDT_INH	EMU_WDT_INH
FCLK_IN	FCLK_TEMP	FCLK_IN

FWE_IN	FWE_IN	FWE_IN
INT_N	INT	INT
KBD_CLOSE	KBD_CLOSE	KBD_CLOSE
KBD_WAND_EN	KBD_WAND_EN	KBD_WAND_EN
LED_ON	LED_ON	
MEM_ALE	MEM_ALE	MEM_ALE
NDOE	NDOE	NDOE
N_DOWNLOAD	N_DOWNLOAD	N_DOWNLOAD
N_RS232_REN	N_RS232_REN	N_RS232_REN
N_RS232_TEN	N_RS232_TEN	N_RS232_TEN
N_TG_EN	N_TG_EN	*usb_xmit_out*
OCIA_CLKIN	OCIA_CLKIN	OCIA_CLKIN
OCIA_CLKOUT	OCIA_CLKOUT	OCIA_CLKOUT
OCIA_EN	OCIA_EN	OCIA_EN
OCIA_SDATA	OCIA_SDATA	OCIA_SDATA
P13_IN	P13_IN	P13_IN
P14_IN	P14_IN	P14_IN
P17_IN	P17_IN	P17_IN
P1_OUT_EN(0)	n158	P1_OUT_EN(0)
P1_OUT_EN(1)	n157	P1_OUT_EN(1)
P1_OUT_EN(2)	n156	P1_OUT_EN (2)
P1_OUT_EN(3)	n155	P1_OUT_EN (3)
P1_OUT_EN(4)	n154	P1_OUT_EN (4)
P1_OUT_EN(5)	n153	P1_OUT_EN (5)
P1_OUT_EN(6)	n152	P1_OUT_EN (6)
P1_OUT_EN(7)	n151	P1_OUT_EN (7)
P3_OUT_EN(0)	n166	P3_OUT_EN(0)
P3_OUT_EN(1)	n165	P3_OUT_EN (1)
P3_OUT_EN(2)	n164	P3_OUT_EN (2)
P3_OUT_EN(3)	n163	P3_OUT_EN (3)
P3_OUT_EN(4)	n162	P3_OUT_EN (4)
P3_OUT_EN(5)	n161	P3_OUT_EN (5)
P3_OUT_EN(6)	n160	P3_OUT_EN (6)
P3_OUT_EN(7)	n159	P3_OUT_EN (7)
PLL_ON_OFF	PLL_ON_OFF	PLL_ON_OFF
PORT1_OUT(0)	PORT1_OUT_0_port	PORT1_OUT (0)
PORT1_OUT(1)	PORT1_OUT_1_port	PORT1_OUT (1)
PORT1_OUT(2)	PORT1_OUT_2_port	*PORT1_OUT (2)*
PORT1_OUT(3)	PORT1_OUT_3_port	*PORT1_OUT (3)*
PORT1_OUT(4)	PORT1_OUT_4_port	PORT1_OUT (4)
PORT1_OUT(5)	PORT1_OUT_5_port	PORT1_OUT (5)
PORT1_OUT(6)	PORT1_OUT_6_port	PORT1_OUT (6)
PORT1_OUT(7)	PORT1_OUT_7_port	PORT1_OUT (7)
PORT3_IN(0)	PORT3_IN_0_port	PORT3_IN (0)
PORT3_IN(1)	n169	PORT3_IN (1)
PORT3_IN(2)	PORT3_IN_2_port	PORT3_IN (2)
PORT3_IN(3)	PORT3_IN_3_port	PORT3_IN (3)
PORT3_IN(4)	PORT3_IN_4_port	PORT3_IN (4)
PORT3_IN(5)	PORT3_IN_5_port	PORT3_IN (5)
PORT3_IN(6)	n168	PORT3_IN (6)
PORT3_IN(7)	n167	PORT3_IN (7)
PORT3_IN_1_port <= '1'	Ignore	
PORT3_IN_6_port <= '1'	Ignore	
PORT3_IN_7_port <= '1'	Ignore	
PORT3_OUT(0)	PORT3_OUT_0_port	PORT3_OUT (0)
PORT3_OUT(1)	PORT3_OUT_1_port	PORT3_OUT (1)
PORT3_OUT(2)	PORT3_OUT_2_port	PORT3_OUT (2)
PORT3_OUT(3)	PORT3_OUT_3_port	*PORT3_OUT (3)*

PORT3_OUT(4)	PORT3_OUT_4_port	PORT3_OUT (4)
PORT3_OUT(5)	PORT3_OUT_5_port	PORT3_OUT (5)
PORT3_OUT(6)	PORT3_OUT_6_port	PORT3_OUT (6)
PORT3_OUT(7)	PORT3_OUT_7_port	PORT3_OUT (7)
Q1_OUT	Q1_OUT	Q1_OUT
Q2_OUT	Q2_OUT	Q2_OUT
Q3_OUT	Q3_OUT	Q3_OUT
Q4_OUT	Q4_OUT	Q4_OUT
Q5_OUT	Q5_OUT	Q5_OUT
RD_N	RD	RD
RESET_N	RESET	RESET
RES_IN	RES_IN	RESISTORS_IN
RS232_IN1	RS232_IN1	RS232_IN1
RS232_IN2	RS232_IN2	RS232_IN2
RS232_OUT1	RS232_OUT1	RS232_OUT1
RS232_OUT2	RS232_OUT2	RS232_OUT2
RS485_OE	RS485_OE	RS485_OE
RSV1_EN	RSV1_EN	RSV1_EN
RSV1_IN	RSV1_IN	*RSV1_in*
RSV1_OUT	RSV1_OUT	
RXD_BY	RXD_BYPASS	RXD_BY
SCAN_STAND	SCAN_STAND	SCAN_STAND
SOF	SOF_TOGGLE	SOF
SUSPEND	SUSPEND_TEMP	SUSPEND
SYN_EN	SYN_EN	SYN_EN
TEST	TEST_IN	TEST
TXD_BY	TXD_BYPASS	TXD_BY
USB_CONN	USB_CONN	USB_CONN
USB_SUSPEND	USB_SUSPEND	USB_SUSPEND
WR_N	WR	wr
		p12_in
		p15_in
		p12_out
		rsv2_en
		dma_ack_en
		dma_req_en

ICE	PROD	I/O	Analog
Used	Used	I	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Used	I	
Used	Used	I	A
Used	Used	I	A
Used	Used	I	A
Used	Not-Used	O	
		o	
		o	
		o	
		o	
		o	
		o	
		o	
		o	
		o	
Used	Used	O	
Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Used	O	A
Used	Used	I	
Used	Used	I	A
Used	Used	I	A
Used	Used	I	A
Used	Used	I	
Used	Used	O	
Used	Used	O	A
Used	Used	O	A
Not-Used	*Not-Used*	O	
Used	Used	I	

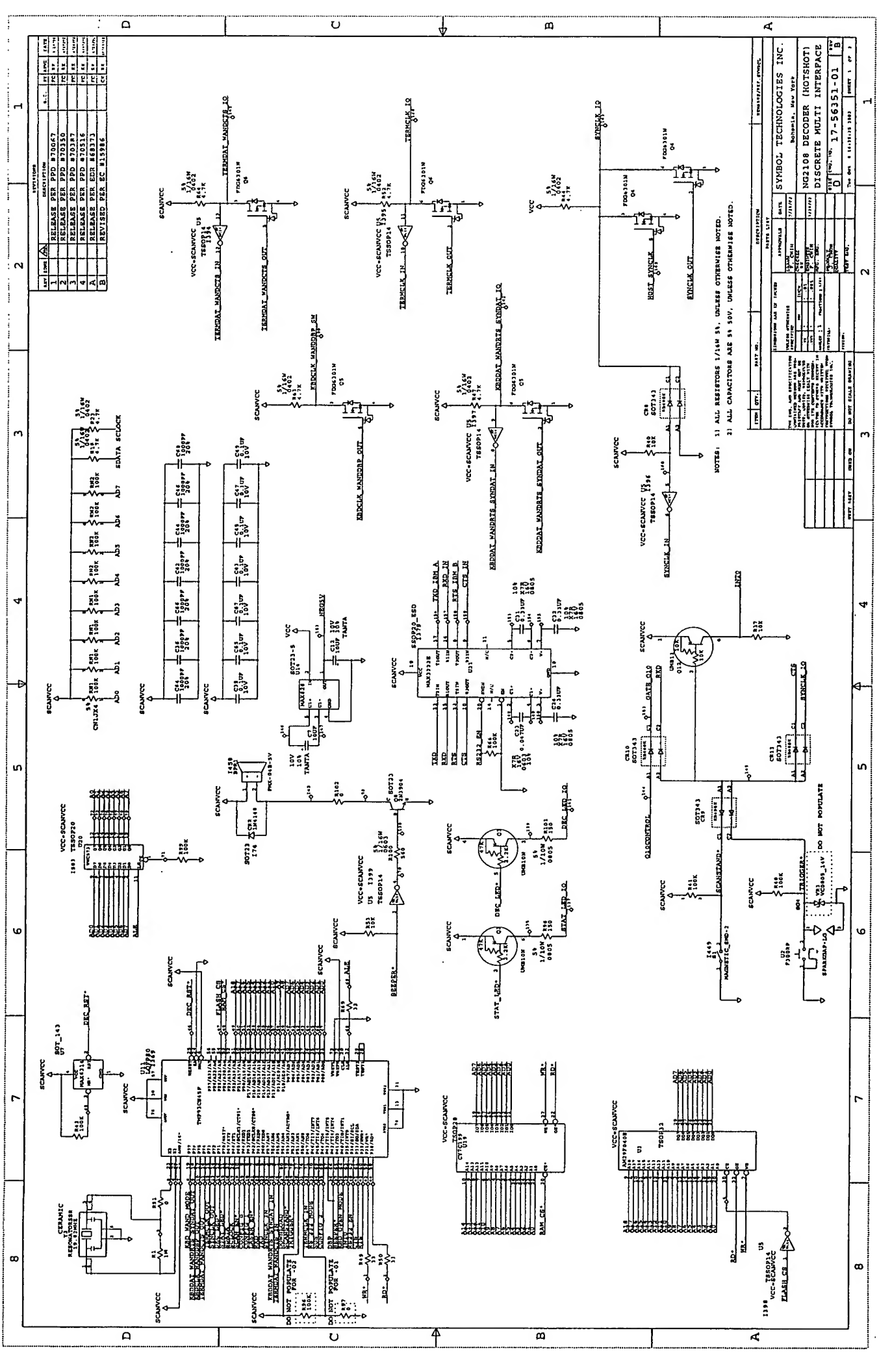
What are these ?
DMA_ACK_SDCI_CLK_IN
DMA_ACK_EN
DMA_REQ_EN
EMU_P11_IN
EMU_P16_IN
EMU_P31_IN
P12_IN
P12_OUT
P15_IN

Used	Used	I	
Used	Used	I	
Used	Used	I	
Used	Used	I	
Used	Used	I	
Used	Used	I	
Used	Used	I	
Used	Used	O	
Used	Used	O	
Used	Used	O	
Used	Used	O	
Used	Used	O	
Used	Used	O	
Used	Used	O	
Used	Used	O	
Used	Used	O	
Used	Not-Used	O	
Used	0	I	but was incorrect
Used	Used	O	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	0	I	
Used	1	I	
Used	1	I	
0	0	I	
Used	0	I	
0	0	I	
0	0	I	
0	0	I	
Used	0	I	
Used	0	I	
0	0	I	
0	0	I	
Used	0	I	
0	0	I	
0	0	I	
0	0	I	
0	0	I	
0	0	I	
0	0	I	
Used	1	I	
Used	Used	O	
Used	0	I	
Used	Used	I	A

Used	Used	I	
Used	Used	O	
Used	Used	O	A
Used	Used	O	A
Not-Used	*Not-Used*	O	
Used	Not-Used	O	
Used	Used	O	A
Used	Used	I	
Used	Used	O	A
Used	Used	O	A
Used	Used	O	A
Used	Used	I	A
Used	Used	I	A
Used	Used	O	A
Used	Used	I	A
Used	0	I	
Used	Not-Used	O	
Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Used	O	A
Not-Used	Not-Used	O	
Used	Not-Used	O	
Used	*Used*	O	
Used	*Used*	O	
Not-Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Not-Used	O	

Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Not-Used	Not-Used	O	
Used	Used	O	A
Used	Used	O	A
Used	Used	O	A
Used	Used	O	A
Used	Used	O	A
Used	Used	I	
Used	Used	I	
Used	Used	O	A
Used	Used	I	A
Used	Used	I	A
Used	Used	O	A
Used	Used	O	A
Used	Used	O	A
Used	Used	O	
Not-Used	*Not-Used*	*o*	
Used	Used	O	
Used	Used	i	
Used	Used	o	
Used	Used	O	
Used	Used	O	
Used	Used	i	
Used	Used	I	
Used	Used	o	a
Used	Used	O	A
Used	Used	i	
Used	Used	i	
Used	Used	i	
Used	not-used	o	
Used	Used	o	
Used	Used	o	
Used	Used	o	

EXHIBIT CC


SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01
REVISIONS
RELEASE PER PPD #700667
RELEASE PER PPD #701350
RELEASE PER PPD #701387
RELEASE PER PPD #701516
RELEASE PER ECR #69373
RELEASE PER ECC #13986
REVISED PER ECC #13986
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.
DO NOT POPULATE
SCANVCC
VCC-SCANVCC
IRDAT_MANDCTR_IO
IRDAT_MANDCTR_IN
IRDAT_MANDCTR_OUT
TERMCLK_IO
TERMCLK_IN
TERMCLK_OUT
KBDCLK_MANDDRP_EN
KBDCLK_MANDDRP_IO
KBDCLK_MANDDRP_OUT
KBDDAT_MANDRTR_SYNDAT_IO
KBDDAT_MANDRTR_SYNDAT_IN
KBDDAT_MANDRTR_SYNDAT_OUT
SYNCLK_IO
SYNCLK_IN
SYNCLK_OUT
HOST_SYNCLK
SDATA
SCLOCK
TXD_XBM_A
RXD_IN
RTS_IN_B
CTS_IN
DEC_LED_IO
STAT_LED_IO
BEEPER
INTO
FLASH_CE
RAM_CE
MAGNETIC_SWD-2
SPARKDAP-10

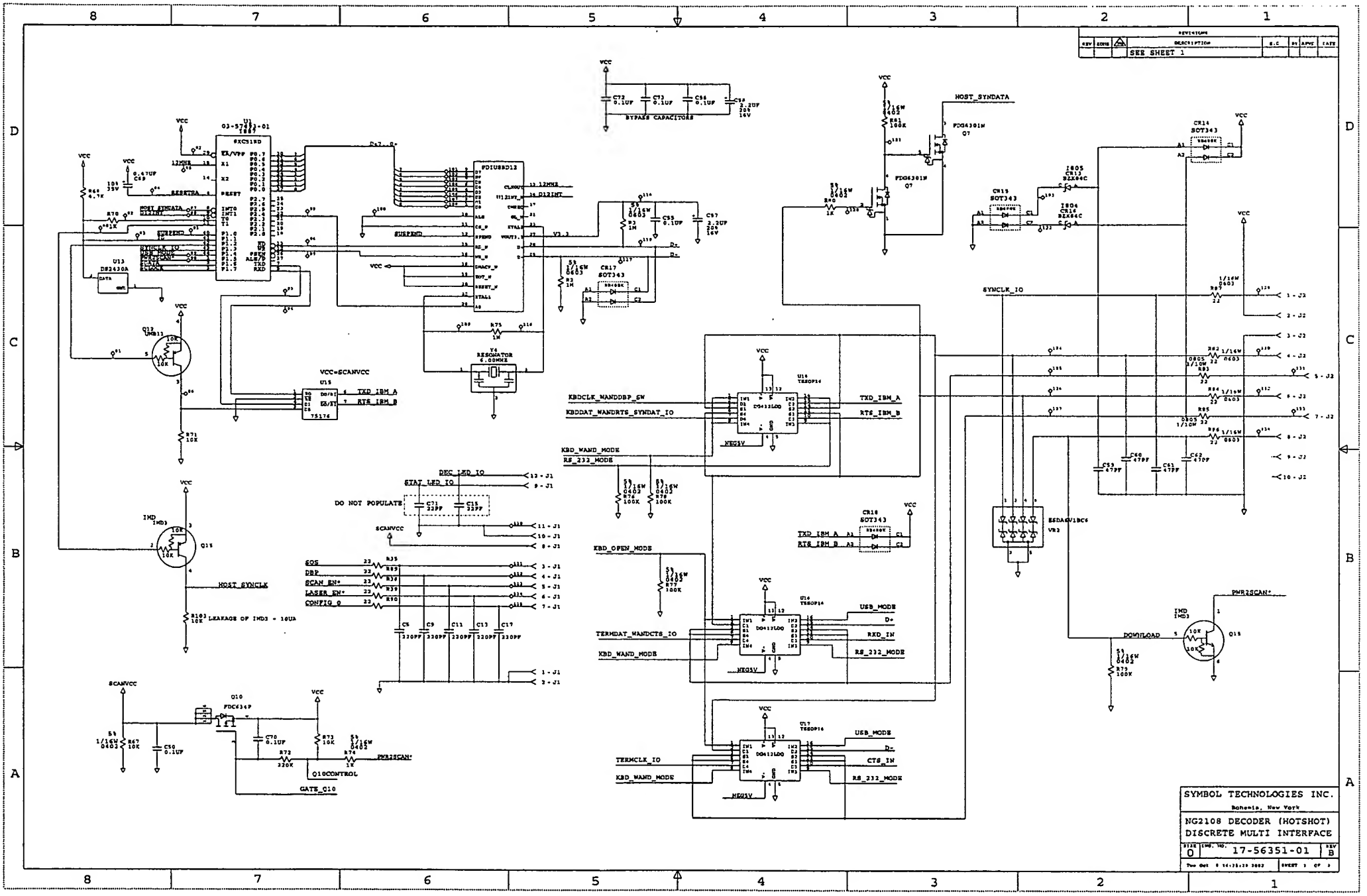
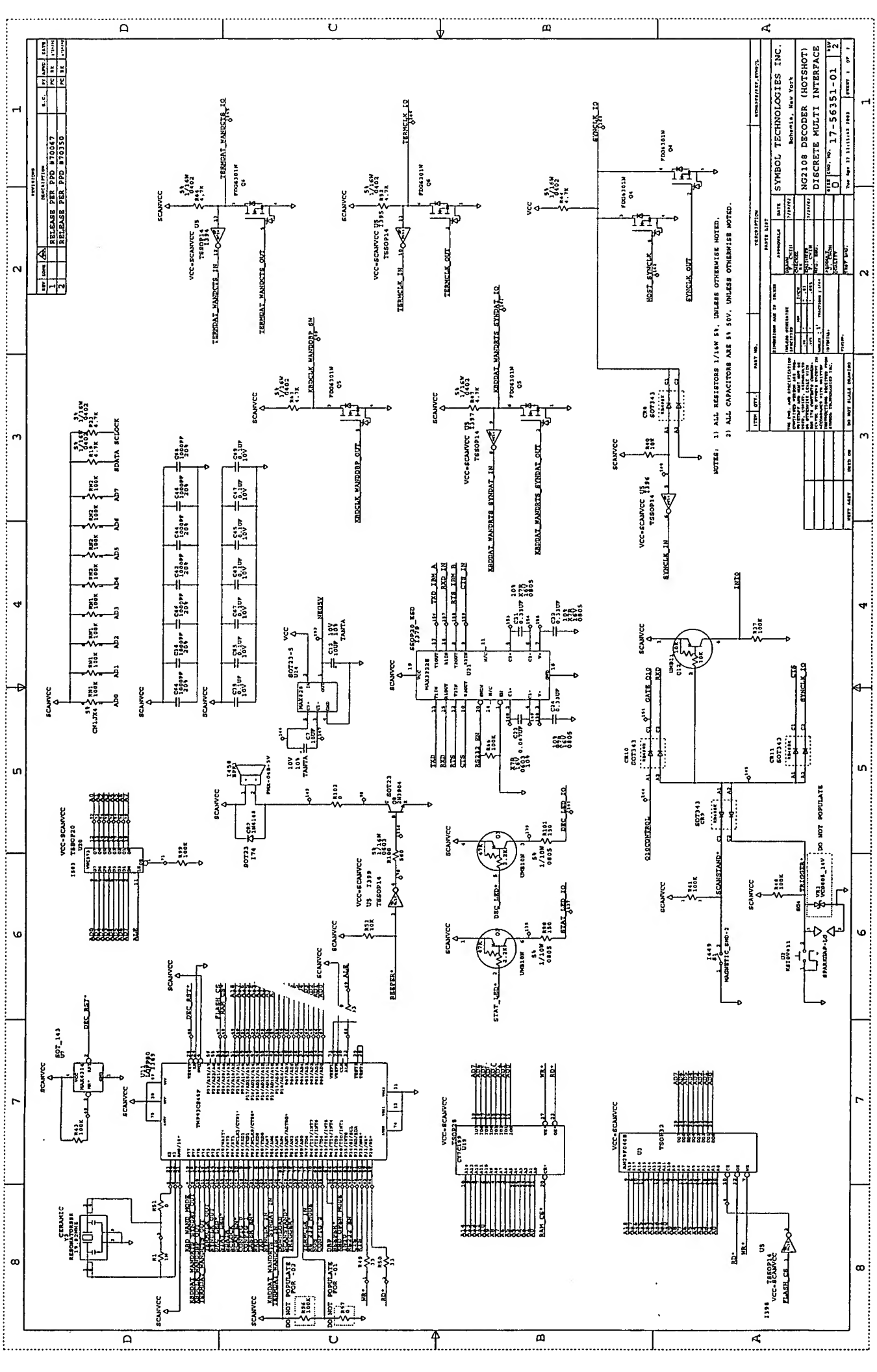

SEE SHEET 1
BYPASS CAPACITORS
HOST_SYNDATA
SYNCLK_IO
KBDCLK_WANDDBP_SW
KBDDAT_WANDRTS_SYNDAT_IO
TXD_IBM_A
RTS_IBM_B
KBD_WAND_MODE
RS_232_MODE
KBD_OPEN_MODE
TERMDAT_WANDCTS_IO
USB_MODE
RXD_IN
TERMCLK_IO
CTS_IN
SUSPEND
HOST_SYNCLK
DOWNLOAD
PWR2SCAN*
Q10CONTROL
GATE_Q10
SCANVCC
REC_LED_IO
STAT_LED_IO
DO NOT POPULATE
LEAKAGE OF IMD3 = 10UA
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01

EXHIBIT DD


SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.
DO NOT POPULATE
DO NOT POPULATE FOR -02
SCANVCC
VCC
SCLOCK
SDATA
KBDCLK_MANDRP
KBDDAT_MANDRP
KBDCLK_MANDRTS_SYNDAT
KBDDAT_MANDRTS_SYNDAT
TERMCLK
TERMDAT_MANDCTS
TERMDAT_MANDCTS_IO
TERMCLK_IO
SYNCLK
SYNCLK_IO
HOST_SYNCLK
SYNCLK_OUT
TERMCLK_IN
TERMCLK_OUT
TERMDAT_MANDCTS_IN
TERMDAT_MANDCTS_OUT
KBDCLK_MANDRP_IN
KBDCLK_MANDRP_OUT
KBDDAT_MANDRTS_SYNDAT_IN
KBDDAT_MANDRTS_SYNDAT_OUT
SCANSTAND
TRIGGER
BEEPER
DEC_LED
STAT_LED
DEC_LED_IO
STAT_LED_IO
FLASH_CS
RAM_CS
MAGNETIC_SWD-2
SPEAKSNAP-IO
TXD_IBM_A
RXD_IBM_A
RTS_IBM_B
CTS_IBM_B
TXD
RXD
RTS
CTS
RS232_EN
GATE_CLK
CLKOUTPUT
CERAMIC
RESONATOR8MHZ
15.93MHZ
KBD AND WAND MUX
TERMINAL INTERFACE
MAGNETIC STRIPE READER
FLASH MEMORY
RAM MEMORY
SCANNER INTERFACE
MICROPROCESSOR
SYMBOL TECHNOLOGIES INC.

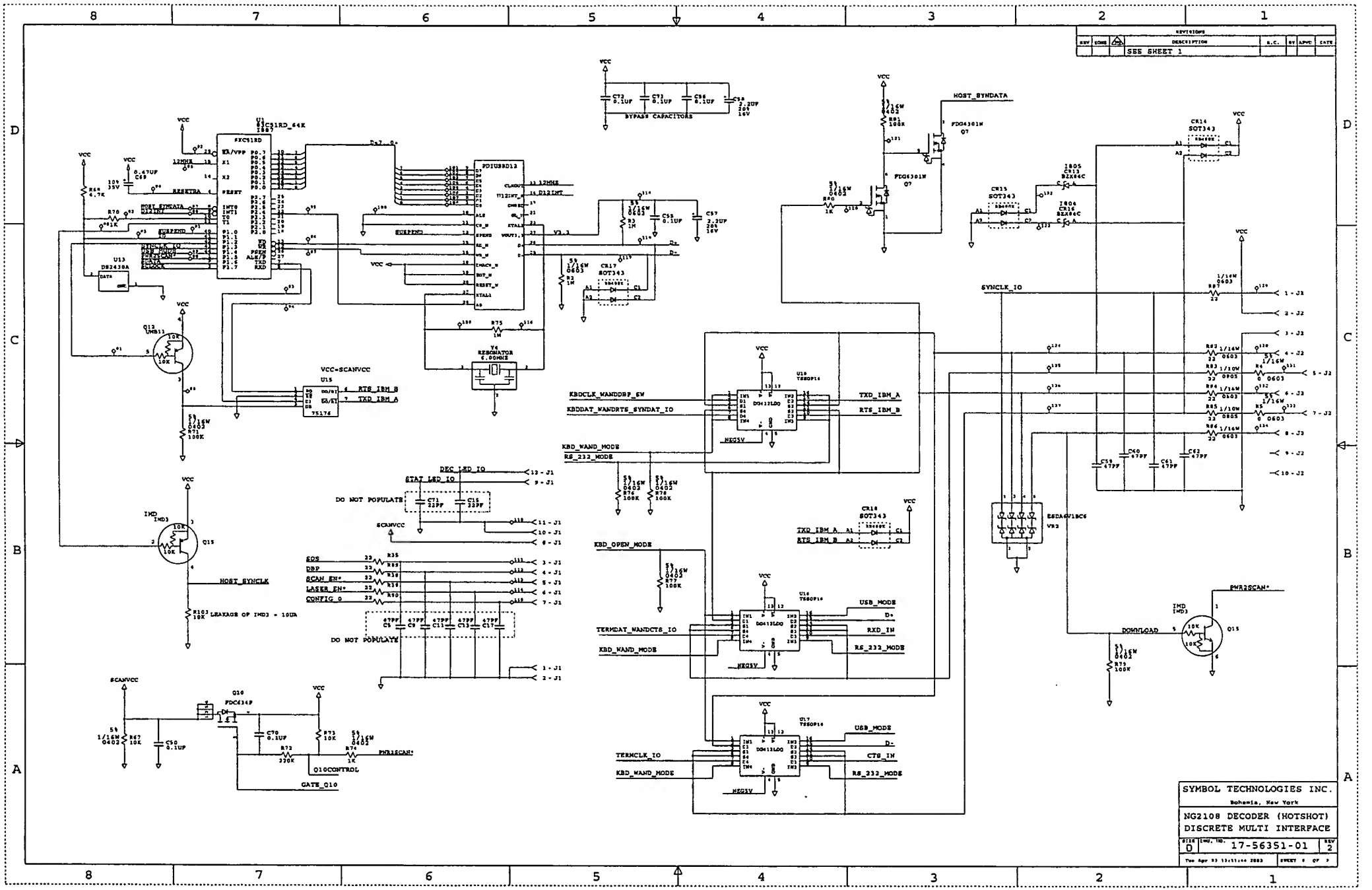
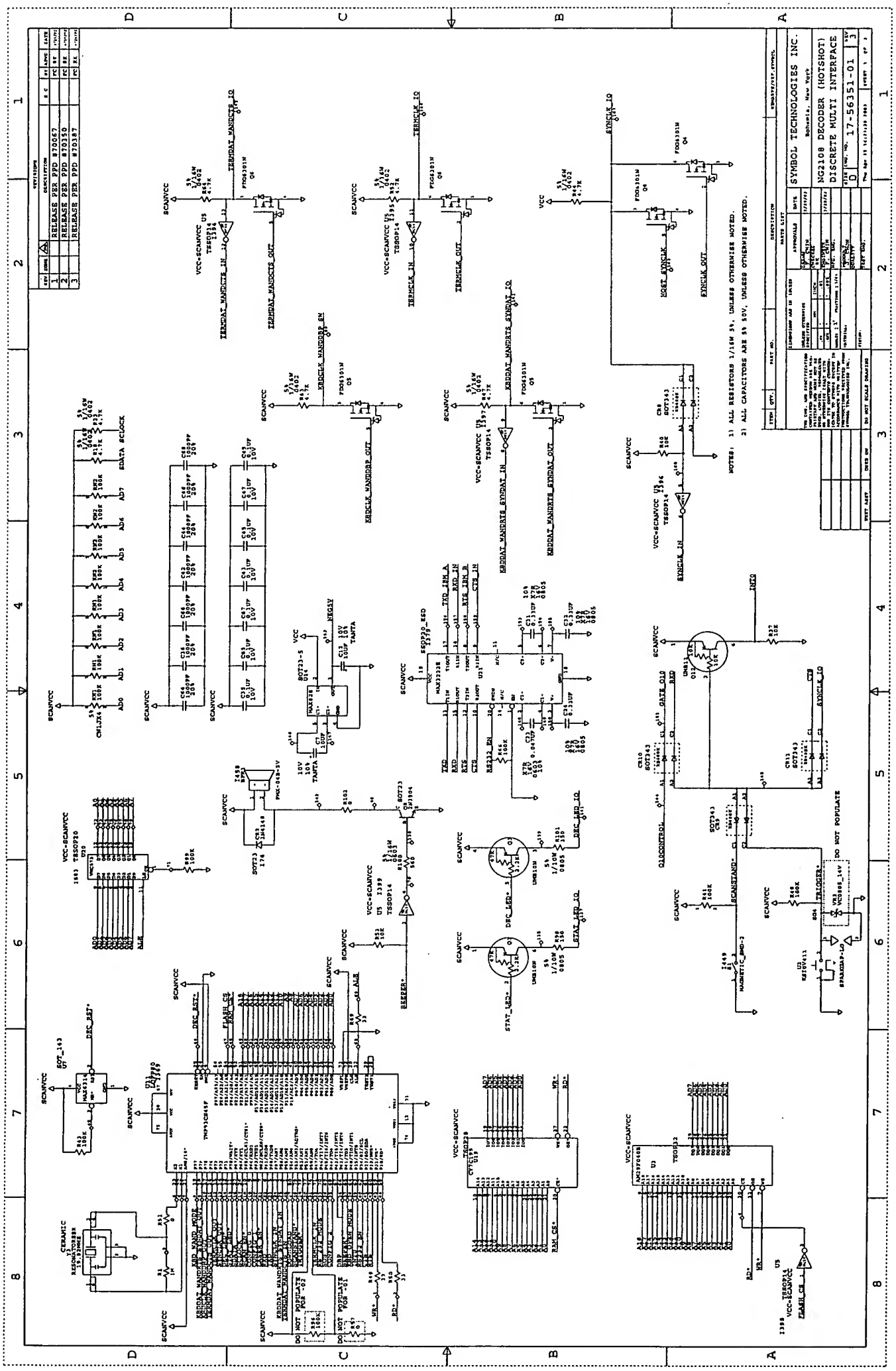

SEE SHEET 1
BYPASS CAPACITORS
HOST_SYNDATA
SYNCLK_IO
KBDCLK_WANDDBP_SW
KBDDAT_WANDRTS_SYNDAT_IO
TXD_IBM_A
RTS_IBM_B
KBD_WAND_MODE
RS_232_MODE
KBD_OPEN_MODE
TERMDAT_WANDCTS_IO
USB_MODE
RXD_IN
TERMCLK_IO
CTS_IN
HOST_SYNCLK
DO NOT POPULATE
DOWNLOAD
PWR2SCAN*
GATE_Q10
Q10CONTROL
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01

EXHIBIT EE


SYMBOL TECHNOLOGIES INC.
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.
DO NOT POPULATE

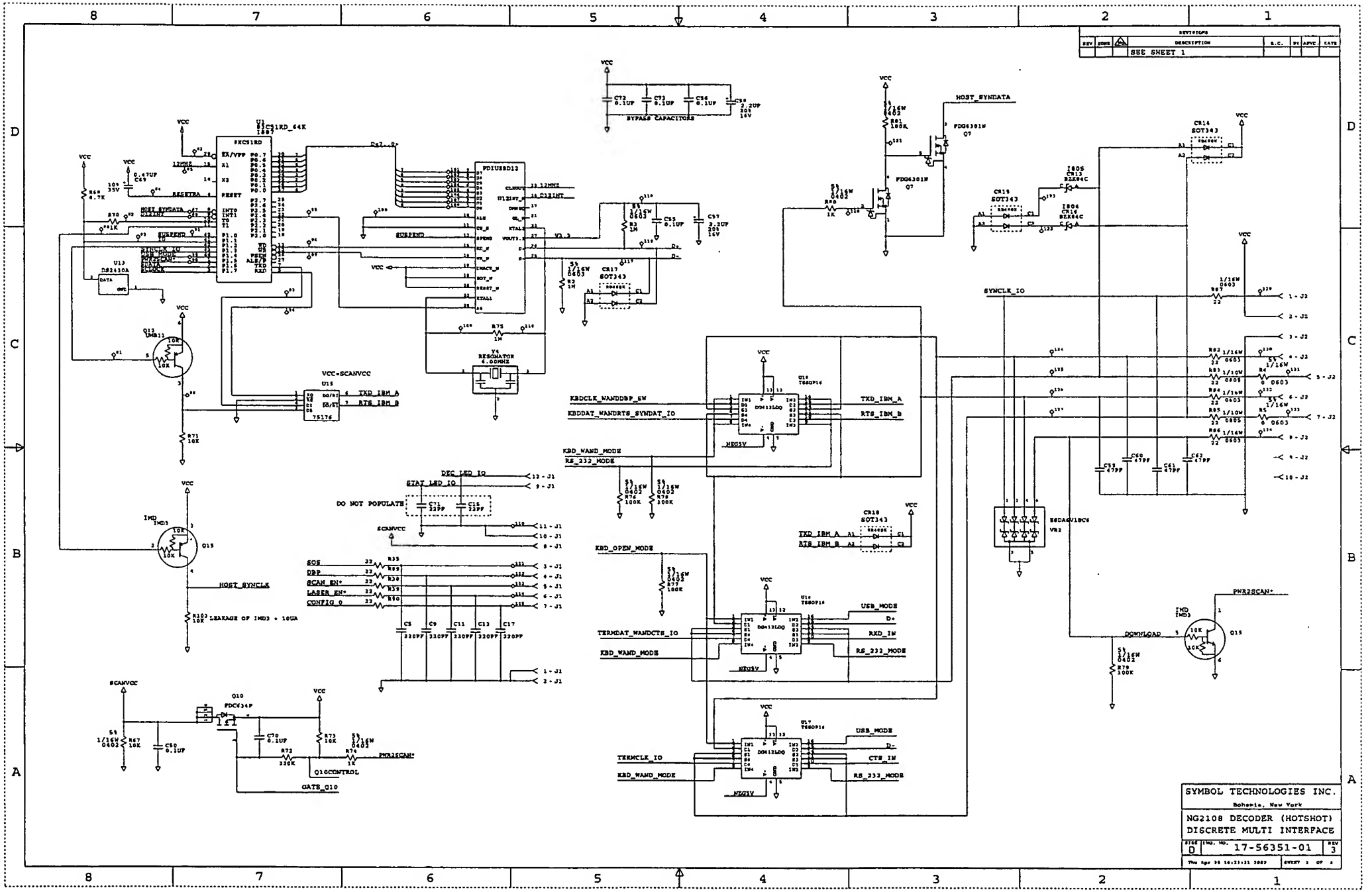
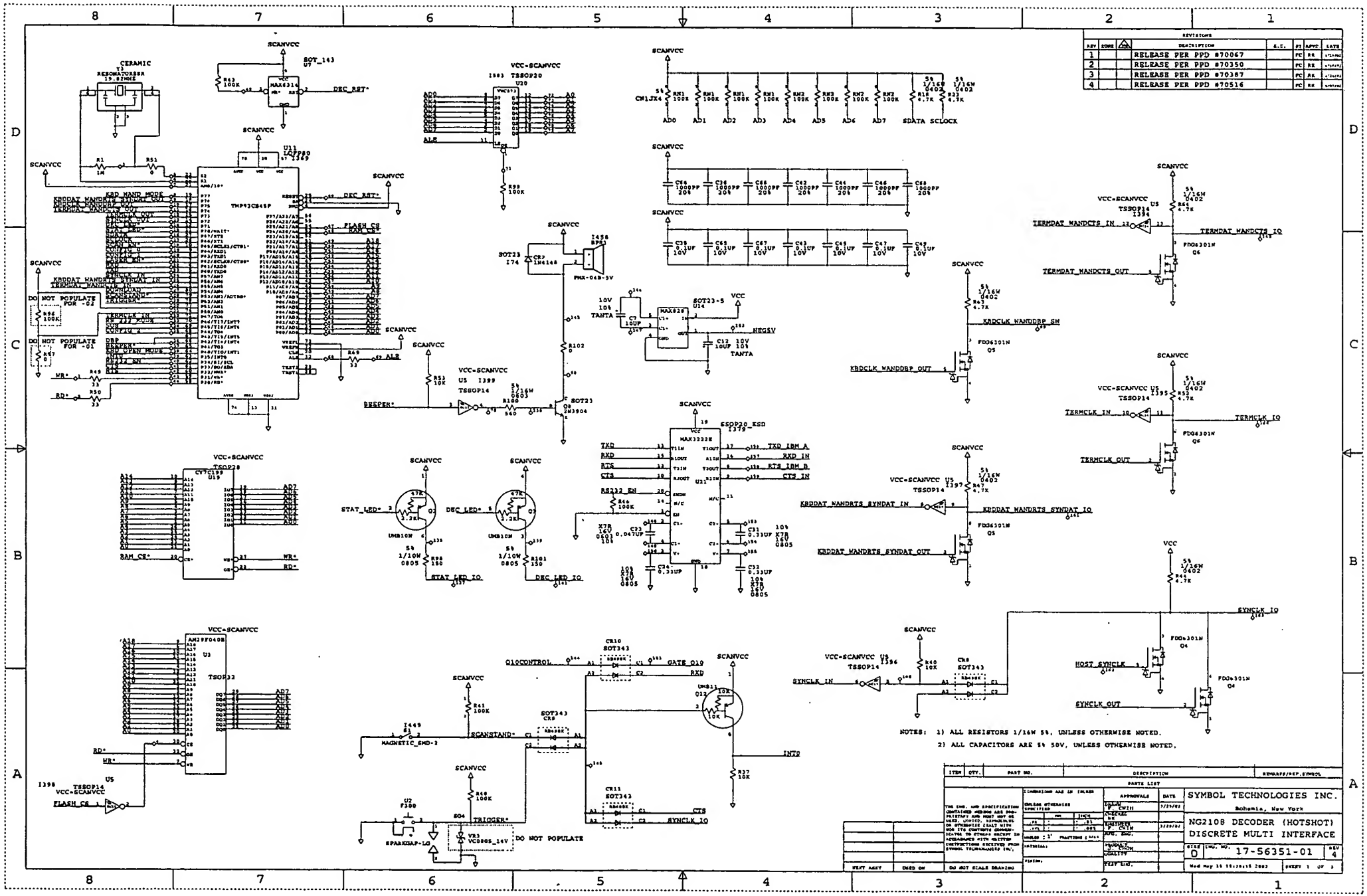

SEE SHEET 1
BYPASS CAPACITORS
HOST_SYNDATA
SYNCLK_IO
SUSPEND
VCC=SCANVCC
TXD_IBM_A
RTS_IBM_B
KBDCLK_WANDDBP_SW
KBDDAT_WANDRTS_SYNDAT_IO
KBD_WAND_MODE
RS_232_MODE
KBD_OPEN_MODE
TERMDAT_WANDCTS_IO
TERMCLK_IO
USB_MODE
RXD_IN
CTS_IN
HOST_SYNCLK
DOWNLOAD
PWR2SCAN*
GATE_Q10
Q10CONTROL
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01

EXHIBIT FF


REVISIONS
REV | ZONE | DESCRIPTION | E.C. | BY | APVD | DATE
1 | | RELEASE PER PPD #70067 | | FC | RR
2 | | RELEASE PER PPD #70350 | | FC | RR
3 | | RELEASE PER PPD #70387 | | FC | RR
4 | | RELEASE PER PPD #70516 | | FC | RR
SCANVCC
VCC-SCANVCC
TMP93CS45F
MAX6314
MAX3222E
TSSOP14
TSSOP28
TSSOP32
SOT23-5
SOT343
FDG6301N
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01

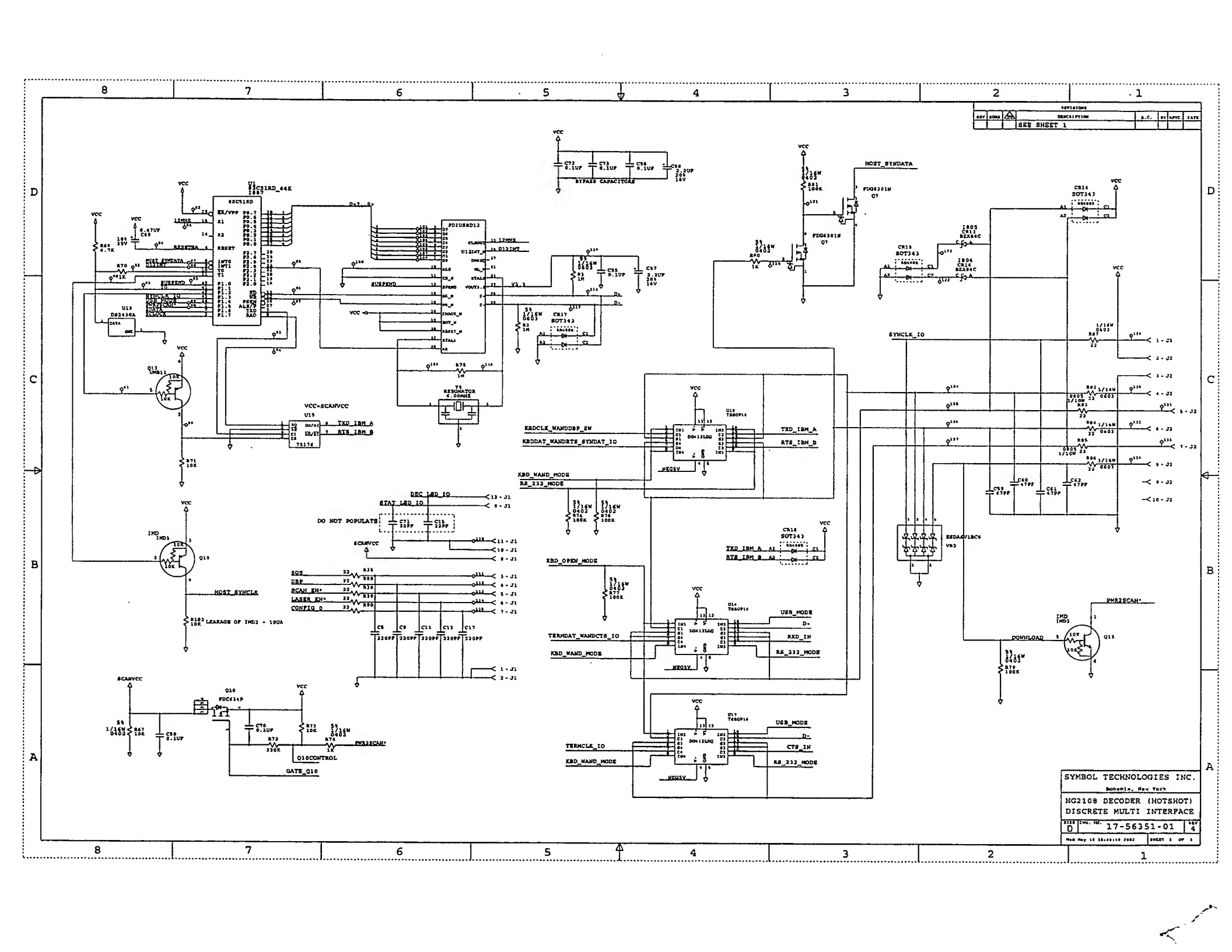
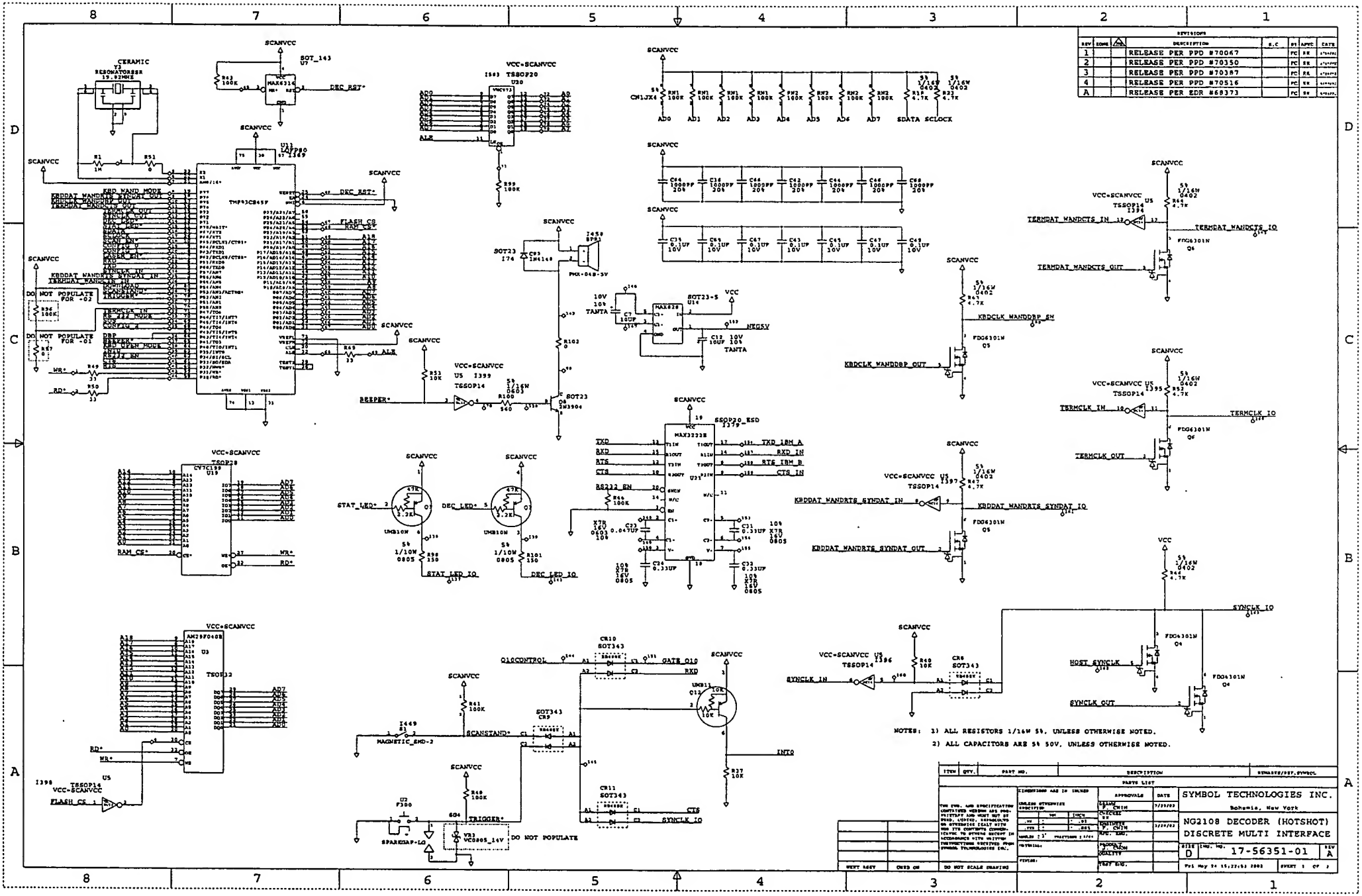

SEE SHEET 1
BYPASS CAPACITORS
HOST_SYNDATA
SUSPEND
6YNCLK_IO
TXD_IBM_A
RTS_IBM_B
KBDCLK_WANDDBP_SW
KBDDAT_WANDRTS_6YNDAT_IO
KBD_WAND_MODE
RS_232_MODE
KBD_OPEN_MODE
TERMDAT_WANDCTS_IO
TERMCLK_IO
USB_MODE
RXD_IN
CTS_IN
HOST_SYNCLK
DEC_LED_IO
STAT_LED_IO
DO NOT POPULATE
SCANVCC
VCC=SCANVCC
Q10CONTROL
GATE_Q10
PWR2SCAN*
DOWNLOAD
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01

EXHIBIT GG


REVISIONS
REV | ZONE | DESCRIPTION | E.C | BY | APVD | DATE
1 | | RELEASE PER PPD #70067 | | FC | RK
2 | | RELEASE PER PPD #70350 | | FC | RK
3 | | RELEASE PER PPD #70387 | | FC | RK
4 | | RELEASE PER PPD #70516 | | FC | RK
A | | RELEASE PER EDR #68373 | | FC | RK
SCANVCC
VCC=SCANVCC
CERAMIC RESONATOR 19.92MHz
MAX6316
DEC_RST*
FLASH_CS
RAM_CS*
KBD MANU MODE
KBDDAT_WANDRTS_SYNDAT_OUT
KBDDAT_WANDRTS_SYNDAT_IN
KBDCLK_WANDDBP_OUT
KBDCLK_WANDDBP_IN
TERMDAT_WANDCTS_OUT
TERMDAT_WANDCTS_IN
TERMCLK_OUT
TERMCLK_IN
SYNCLK_OUT
SYNCLK_IN
HOST_SYNCLK
DO NOT POPULATE FOR -02
DO NOT POPULATE FOR -01
BEEPER*
STAT_LED*
DEC_LED*
STAT_LED_IO
DEC_LED_IO
MAX3222E
TXD
RXD
RTS
CTS
TXD_IBM_A
RXD_IN
RTS_IBM_B
CTS_IN
RS232_EN
Q10CONTROL
GATE_Q10
SCANSTAND*
MAGNETIC_SWD-2
TRIGGER*
SPAREGAP-LG
INT0
DO NOT POPULATE
SDATA
SCLOCK
NEG5V
TANTA
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01
D
A

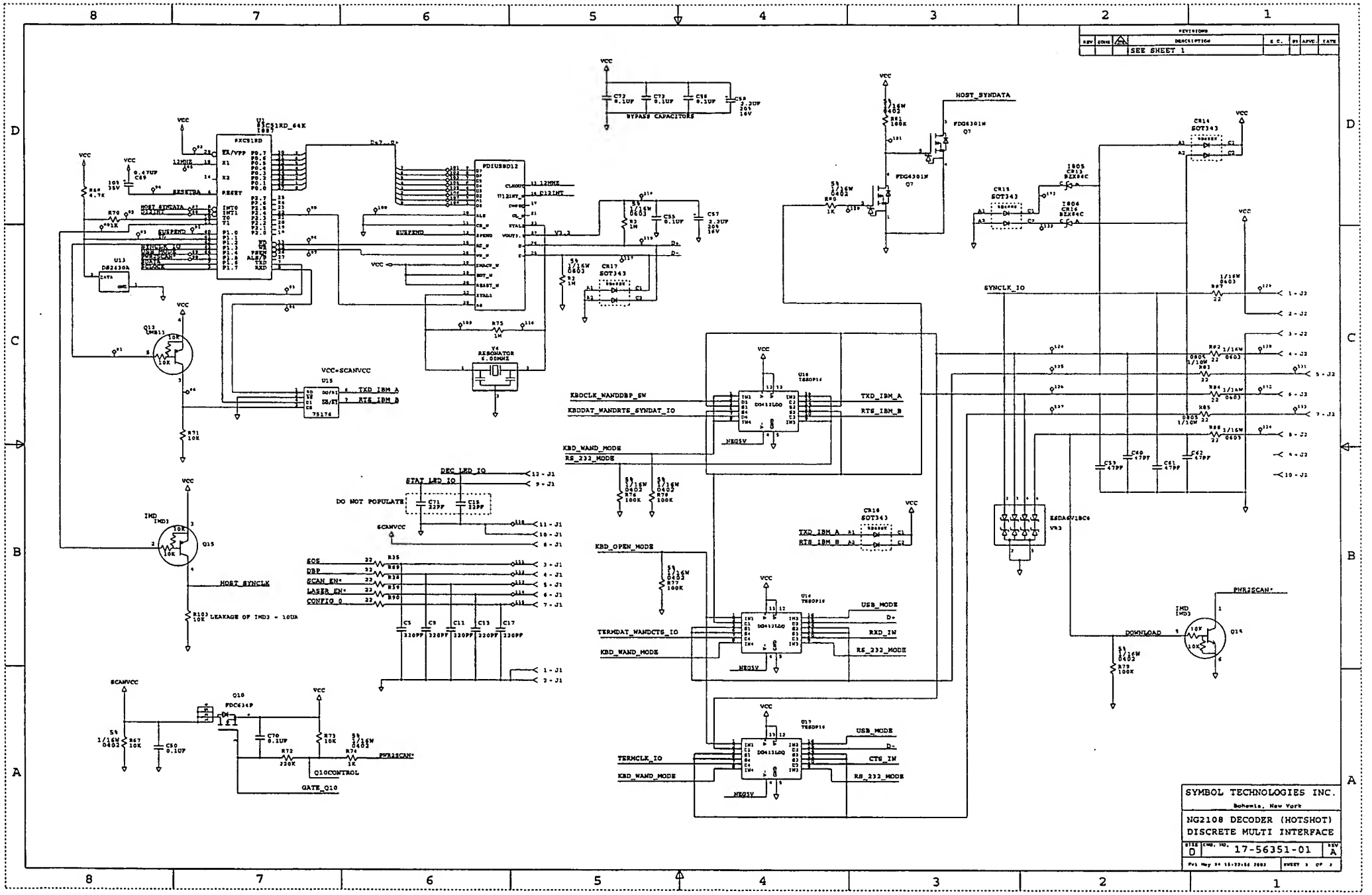

SEE SHEET 1
BYPASS CAPACITORS
HOST_SYNDATA
SYNCLK_IO
KBDCLK_WANDDBP_SW
KBDDAT_WANDRTS_SYNDAT_IO
TXD_IBM_A
RTS_IBM_B
KBD_WAND_MODE
RS_232_MODE
KBD_OPEN_MODE
TERMDAT_WANDCTS_IO
TERMCLK_IO
USB_MODE
RXD_IN
CTS_IN
HOST_SYNCLK
DEC_LED_IO
STAT_LED_IO
DO NOT POPULATE
SCANVCC
Q10CONTROL
GATE_Q10
PWR2SCAN*
DOWNLOAD
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01

EXHIBIT HH

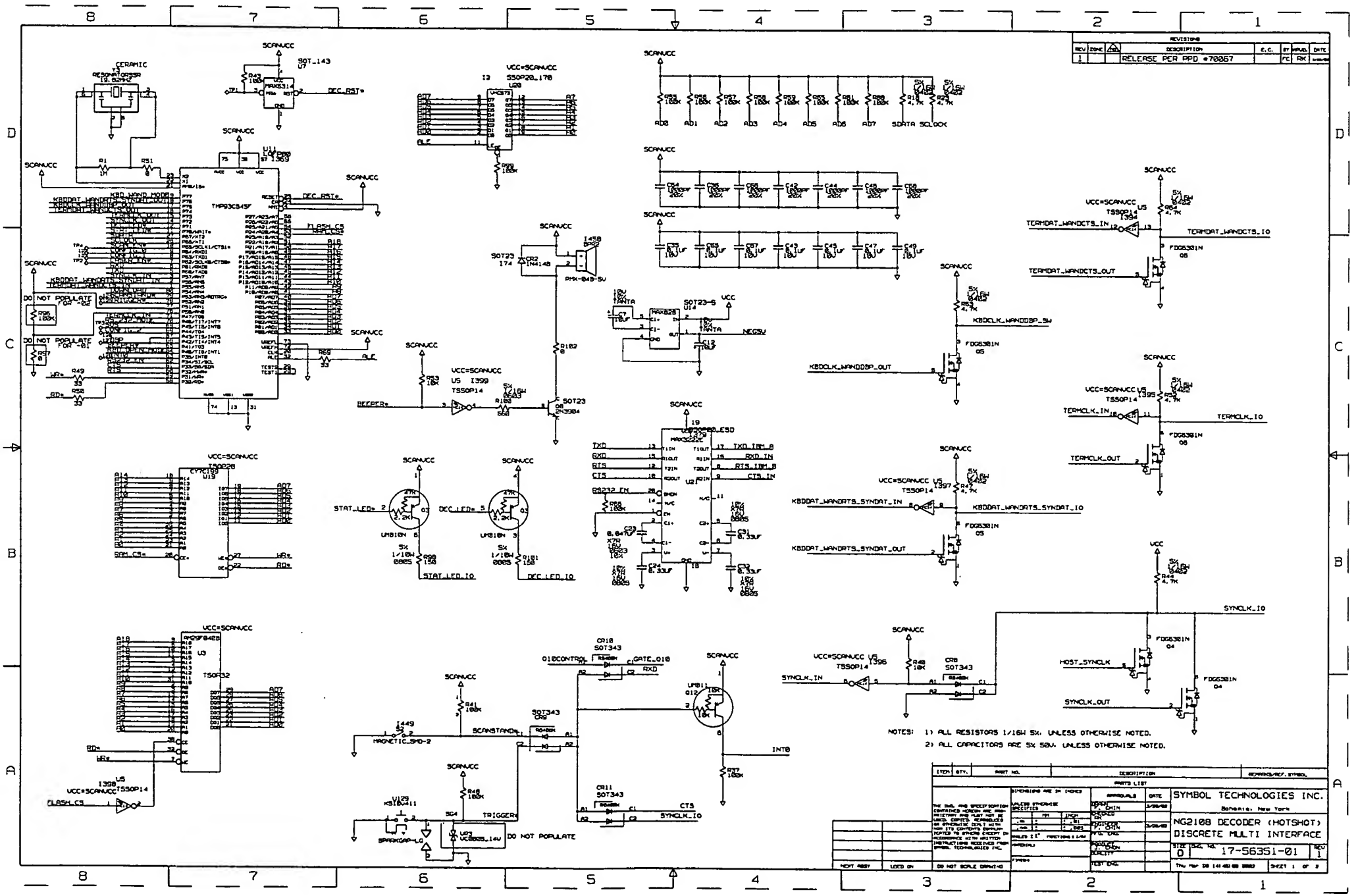

SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01
NOTES: 1) ALL RESISTORS 1/16W 5% UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V. UNLESS OTHERWISE NOTED.

EXHIBIT II

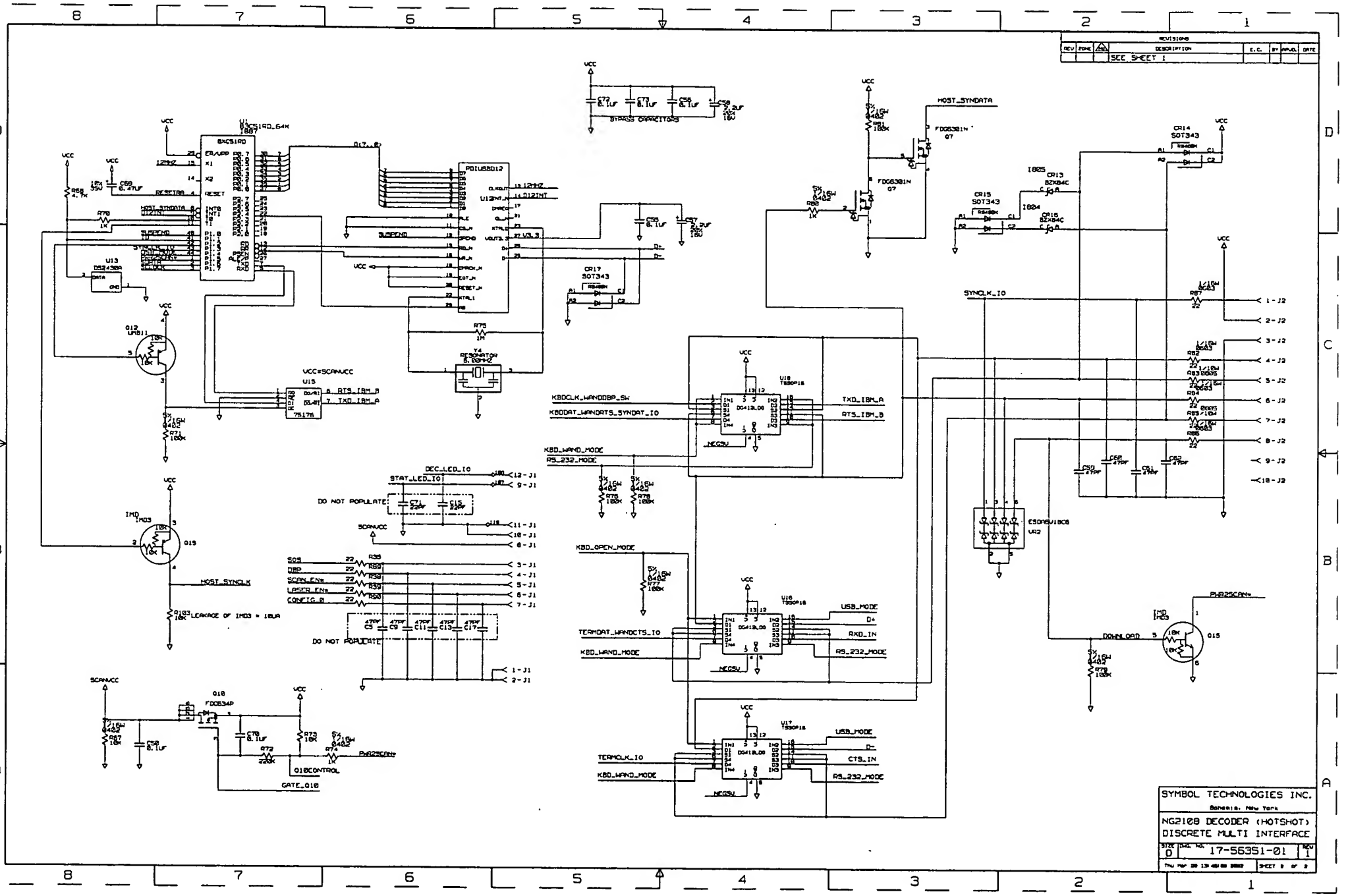
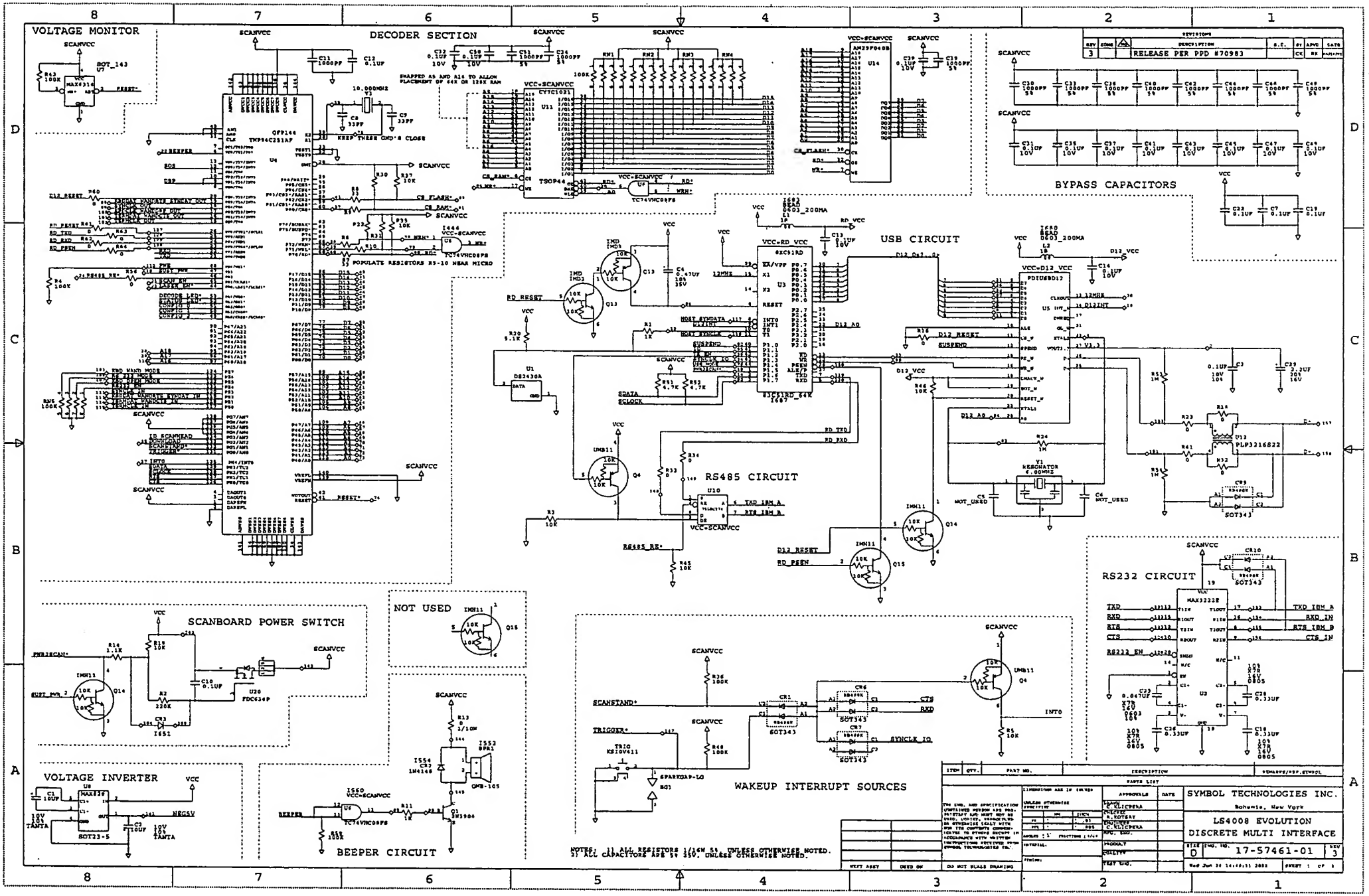

SEE SHEET 1
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
NG2108 DECODER (HOTSHOT)
DISCRETE MULTI INTERFACE
17-56351-01
MOST_SYNDATA
SYNCLK_IO
KBDCLK_WANDDBP_SW
KBDDAT_WANDRTS_SYNDAT_IO
KBD_WAND_MODE
RS_232_MODE
KBD_OPEN_MODE
TERMDAT_WANDCTS_IO
TERMCLK_IO
USB_MODE
TXD_IBM_A
RTS_IBM_B
RXD_IN
CTS_IN
MOST_SYNCLK
DOWNLOAD
SUSPEND
STAT_LED_IO
DEC_LED_IO
SCANVCC
DO NOT POPULATE
LEAKAGE OF IM03 = 18UA
GATE_Q18
Q18CONTROL
PWR2SCAN
ESDA6V1BC6
BYPASS CAPACITORS

EXHIBIT JJ


VOLTAGE MONITOR
DECODER SECTION
BYPASS CAPACITORS
USB CIRCUIT
RS485 CIRCUIT
RS232 CIRCUIT
SCANBOARD POWER SWITCH
NOT USED
VOLTAGE INVERTER
BEEPER CIRCUIT
WAKEUP INTERRUPT SOURCES
RELEASE PER PPD #70983
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01

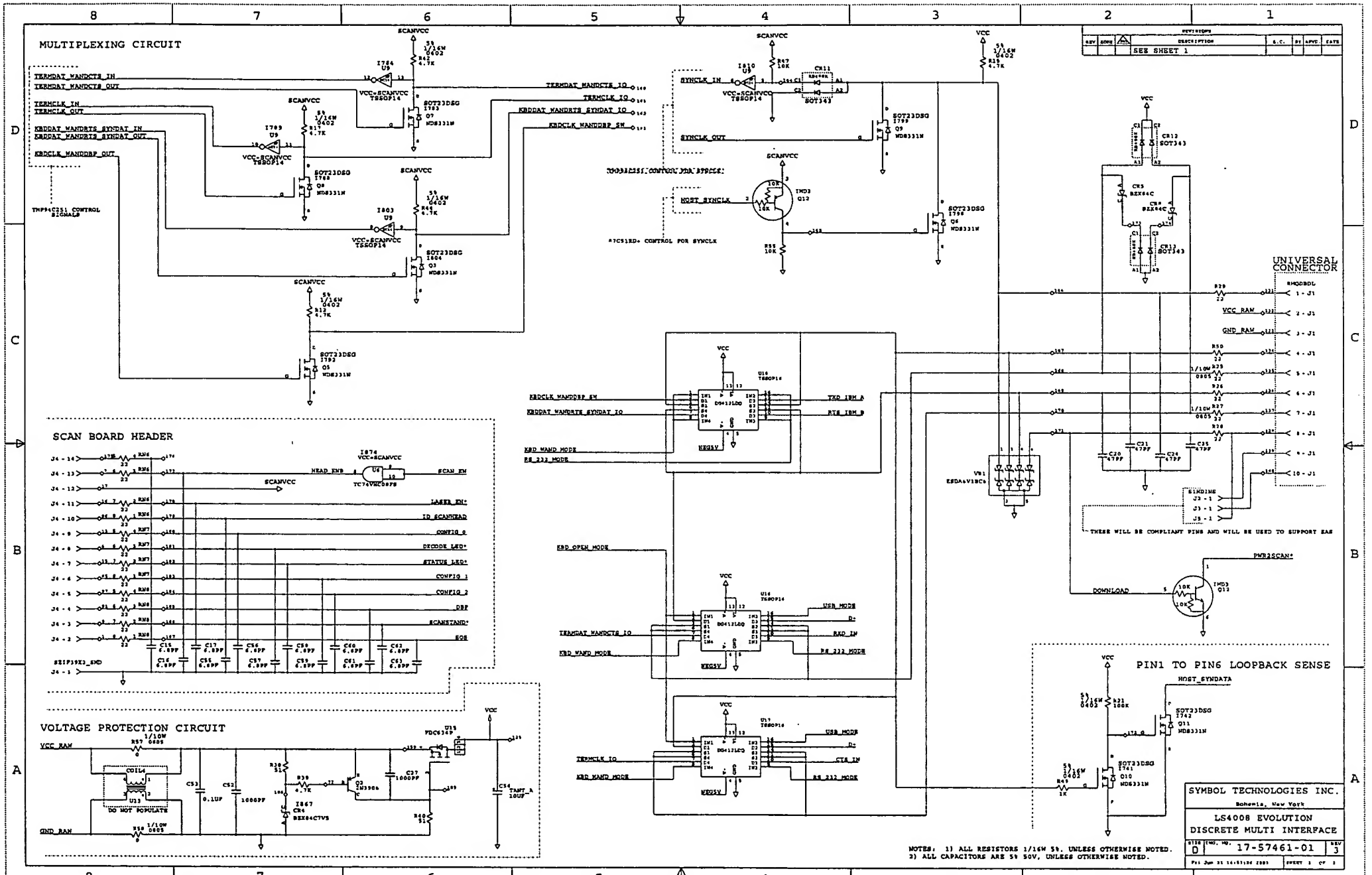
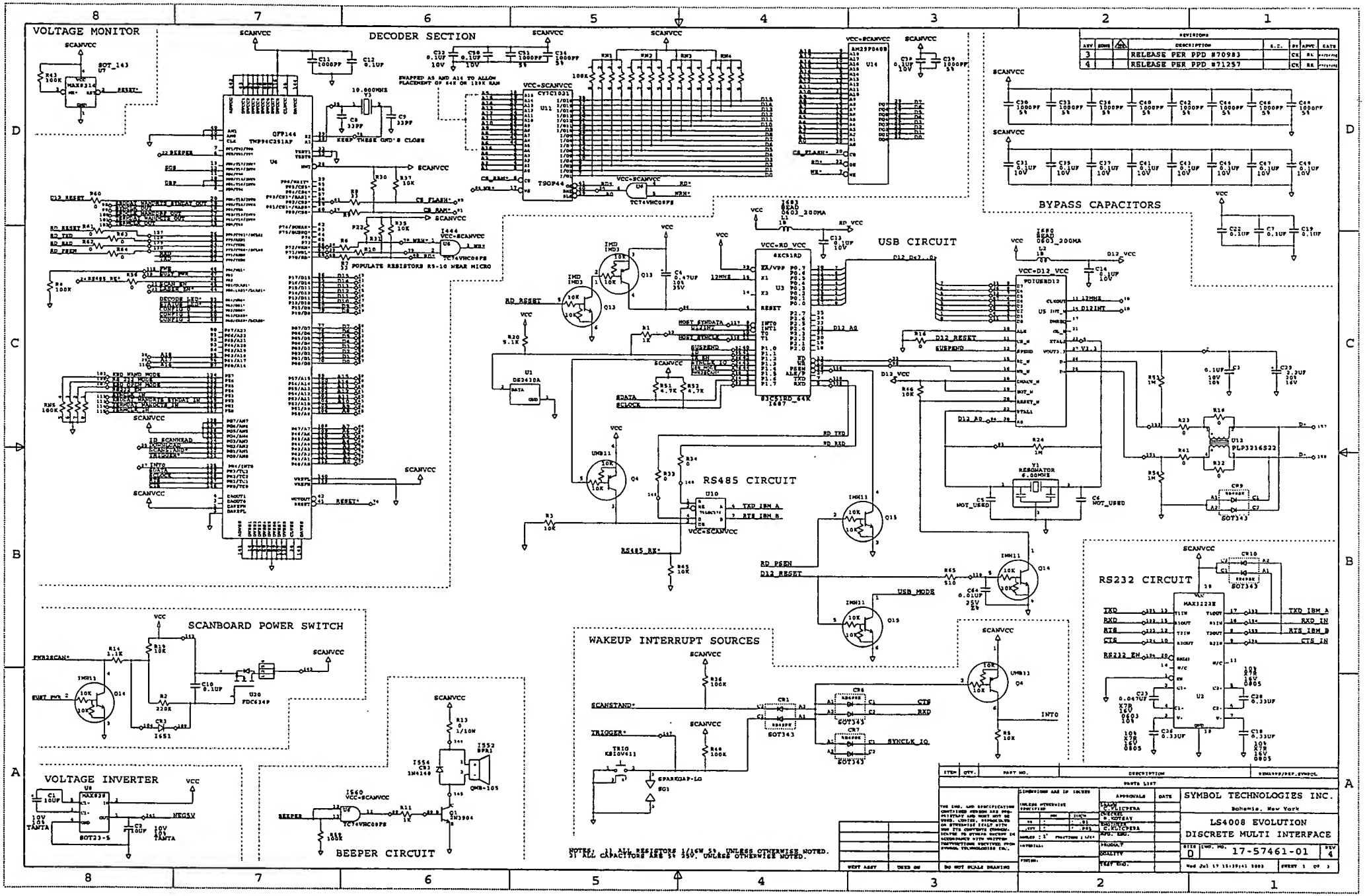

MULTIPLEXING CIRCUIT
SCAN BOARD HEADER
VOLTAGE PROTECTION CIRCUIT
UNIVERSAL CONNECTOR
PIN1 TO PIN6 LOOPBACK SENSE
SEE SHEET 1
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01
NOTES: 1) ALL RESISTORS 1/16W 5%. UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.

EXHIBIT KK


VOLTAGE MONITOR
DECODER SECTION
BYPASS CAPACITORS
USB CIRCUIT
RS485 CIRCUIT
RS232 CIRCUIT
SCANBOARD POWER SWITCH
WAKEUP INTERRUPT SOURCES
VOLTAGE INVERTER
BEEPER CIRCUIT
REVISIONS
RELEASE PER PPD #70983
RELEASE PER PPD #71257
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01

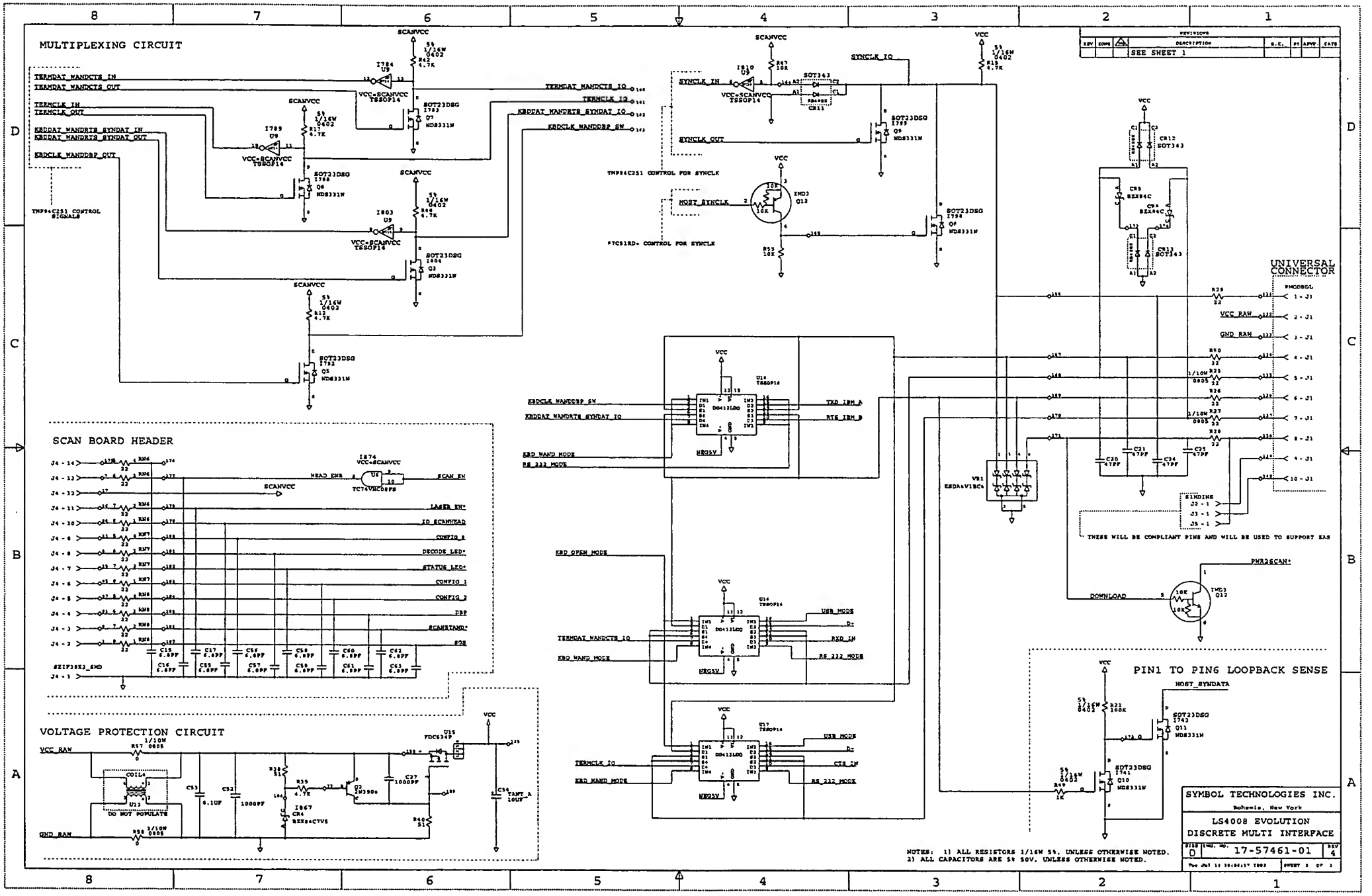
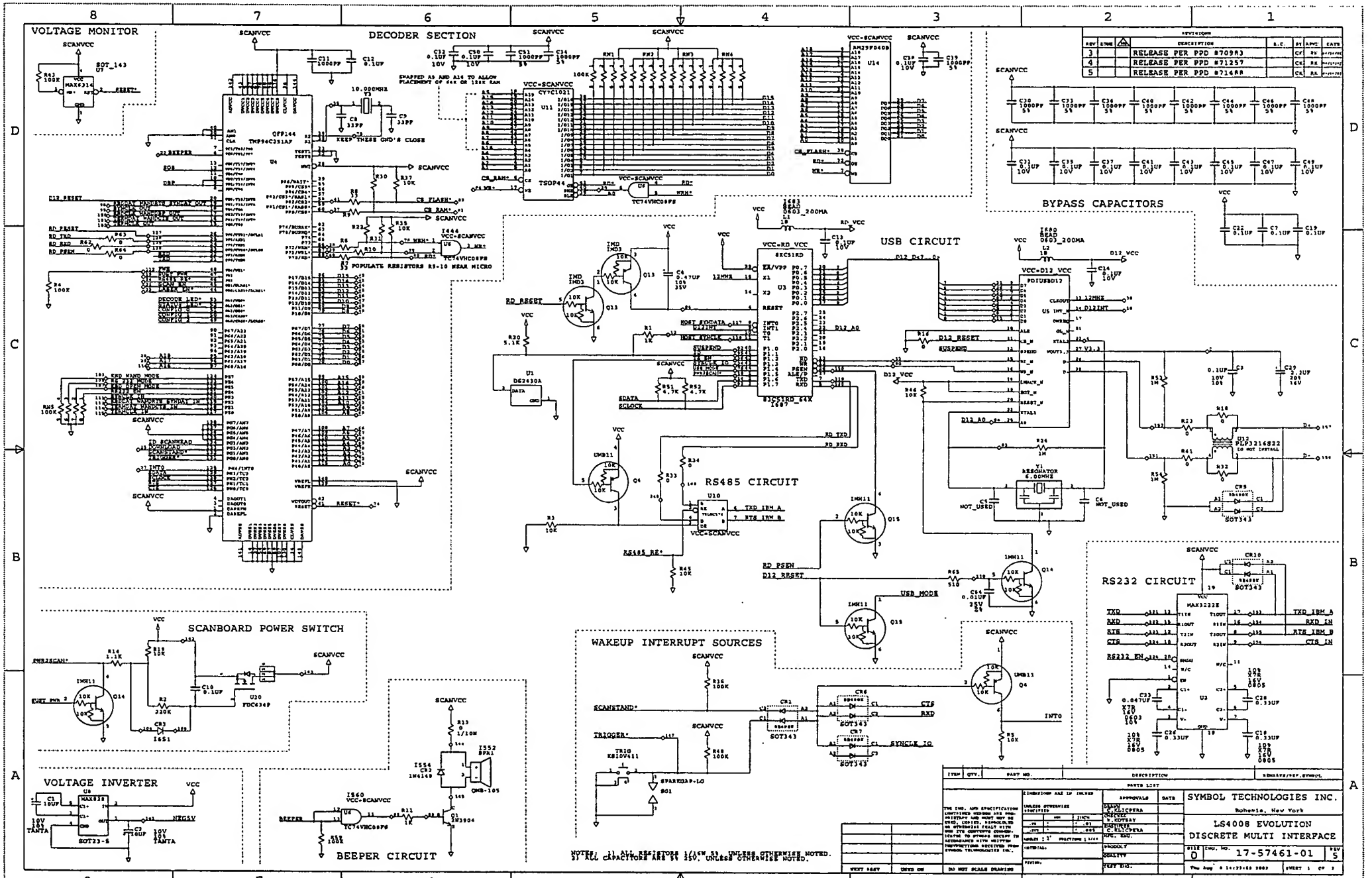

MULTIPLEXING CIRCUIT
SCANVCC
TERMDAT_WANDCTS_IN
TERMDAT_WANDCTS_OUT
TERMCLK_IN
TERMCLK_OUT
KBDDAT_WANDRTS_SYNDAT_IN
KBDDAT_WANDRTS_SYNDAT_OUT
KBDCLK_WANDDBP_OUT
TMP94C251 CONTROL SIGNALS
TERMDAT_WANDCTS_IO
TERMCLK_IO
KBDDAT_WANDRTS_SYNDAT_IO
KBDCLK_WANDDBP_SW
SYNCLK_IN
SYNCLK_OUT
SYNCLK_IO
TMP94C251 CONTROL FOR SYNCLK
HOST_SYNCLK
87C51RD+ CONTROL FOR SYNCLK
VCC
UNIVERSAL CONNECTOR
VCC_RAW
GND_RAW
SCAN BOARD HEADER
SCAN_EN
LASER_EN*
ID_SCANHEAD
CONFIG_0
DECODE_LED*
STATUS_LED*
CONFIG_1
CONFIG_2
DBP
SCANSTAND*
SDR
KBD_WAND_MODE
RS_232_MODE
KBD_OPEN_MODE
TERMDAT_WANDCTS_IO
TERMCLK_IO
TXD_IBM_A
RTS_IBM_B
RXD_IN
CTS_IN
USB_MODE
D+
D-
VOLTAGE PROTECTION CIRCUIT
VCC_RAW
GND_RAW
DO NOT POPULATE
PIN1 TO PIN6 LOOPBACK SENSE
HOST_SYNDATA
DOWNLOAD
THESE WILL BE COMPLIANT PINS AND WILL BE USED TO SUPPORT EAS
SEE SHEET 1
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01

EXHIBIT LL


VOLTAGE MONITOR
DECODER SECTION
BYPASS CAPACITORS
USB CIRCUIT
RS485 CIRCUIT
RS232 CIRCUIT
SCANBOARD POWER SWITCH
WAKEUP INTERRUPT SOURCES
VOLTAGE INVERTER
BEEPER CIRCUIT
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01

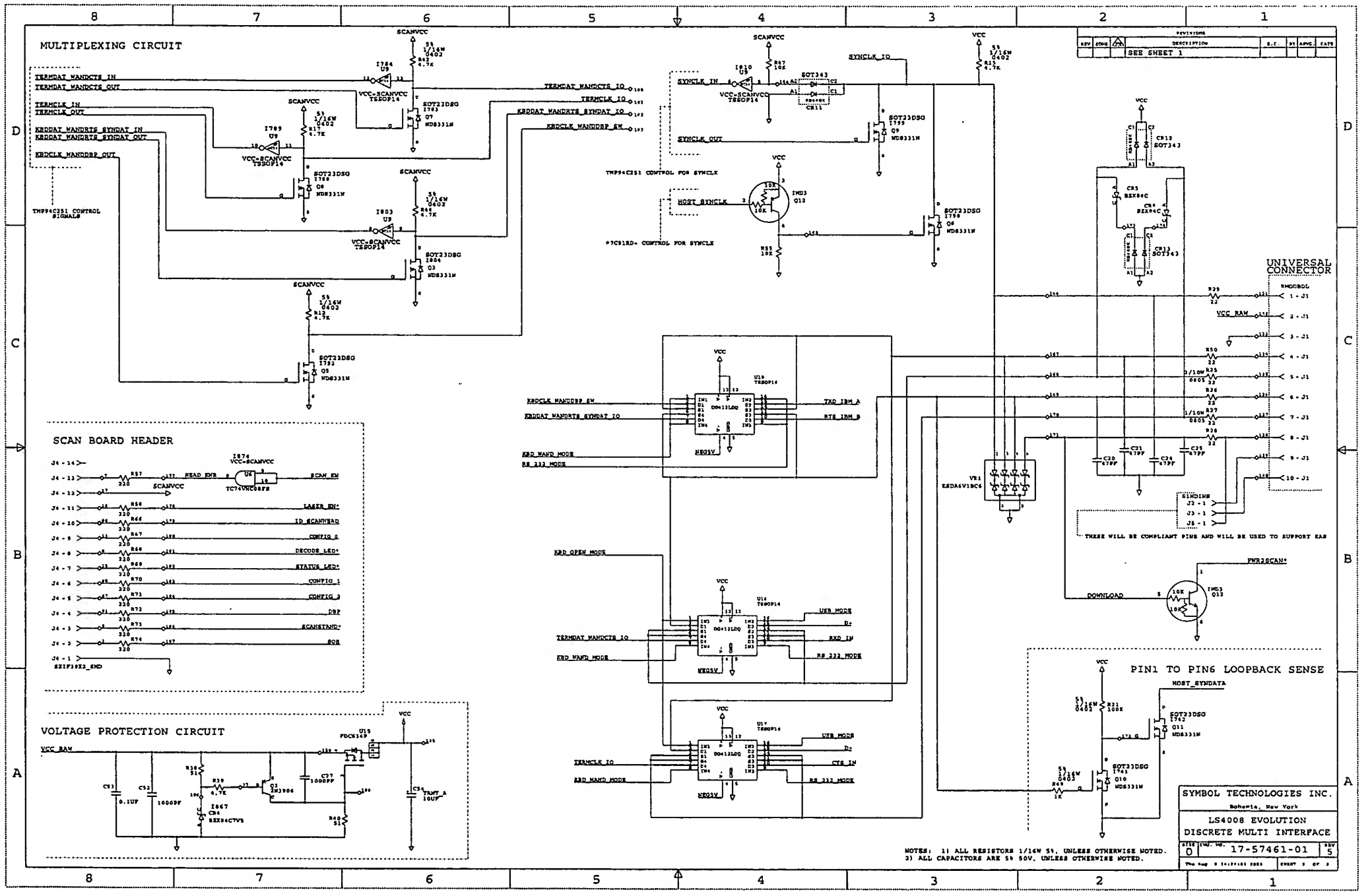
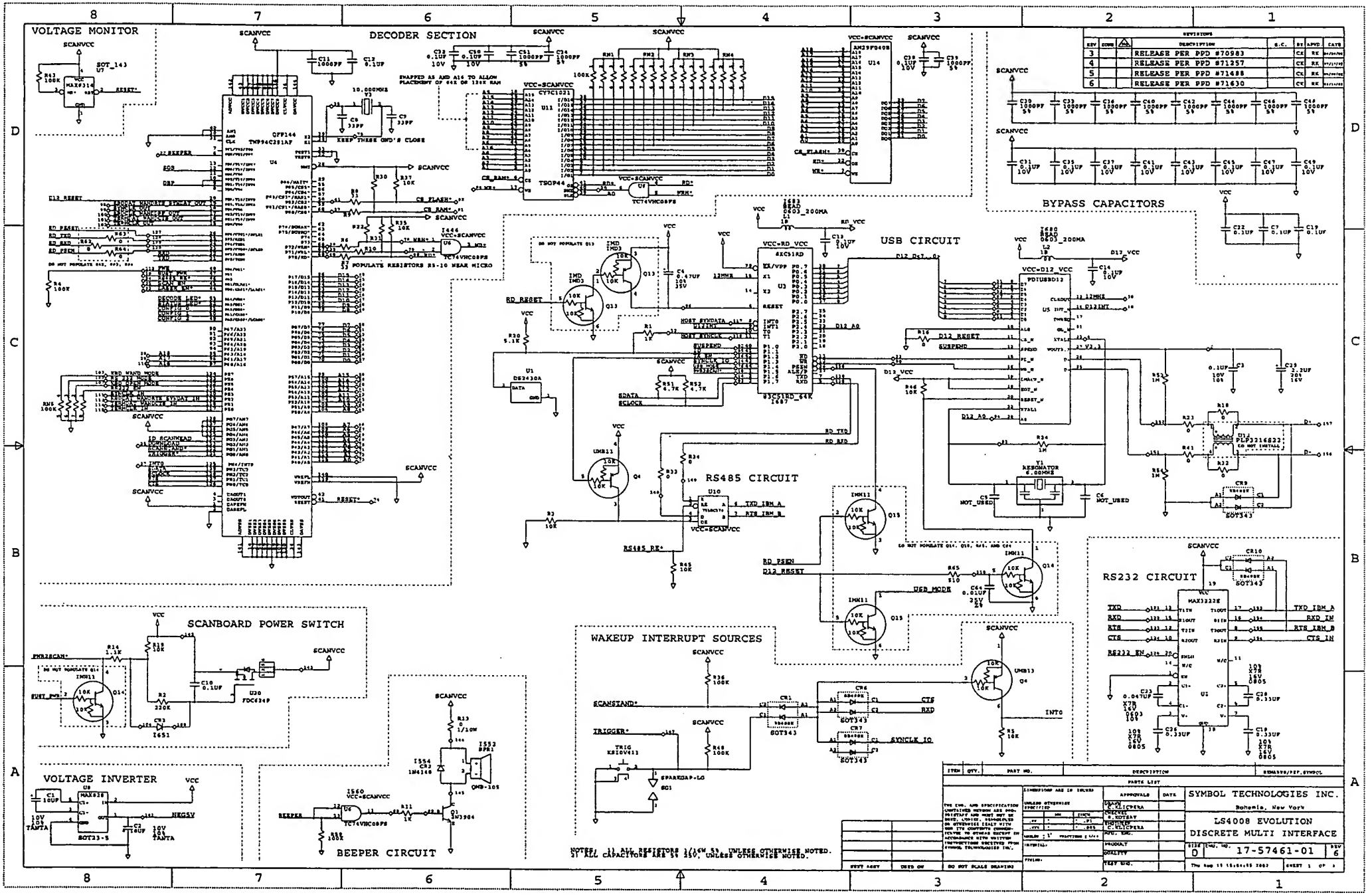

MULTIPLEXING CIRCUIT
SCAN BOARD HEADER
VOLTAGE PROTECTION CIRCUIT
UNIVERSAL CONNECTOR
PIN1 TO PIN6 LOOPBACK SENSE
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V. UNLESS OTHERWISE NOTED.

EXHIBIT MM


VOLTAGE MONITOR
DECODER SECTION
BYPASS CAPACITORS
USB CIRCUIT
RS485 CIRCUIT
SCANBOARD POWER SWITCH
WAKEUP INTERRUPT SOURCES
RS232 CIRCUIT
VOLTAGE INVERTER
BEEPER CIRCUIT
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01

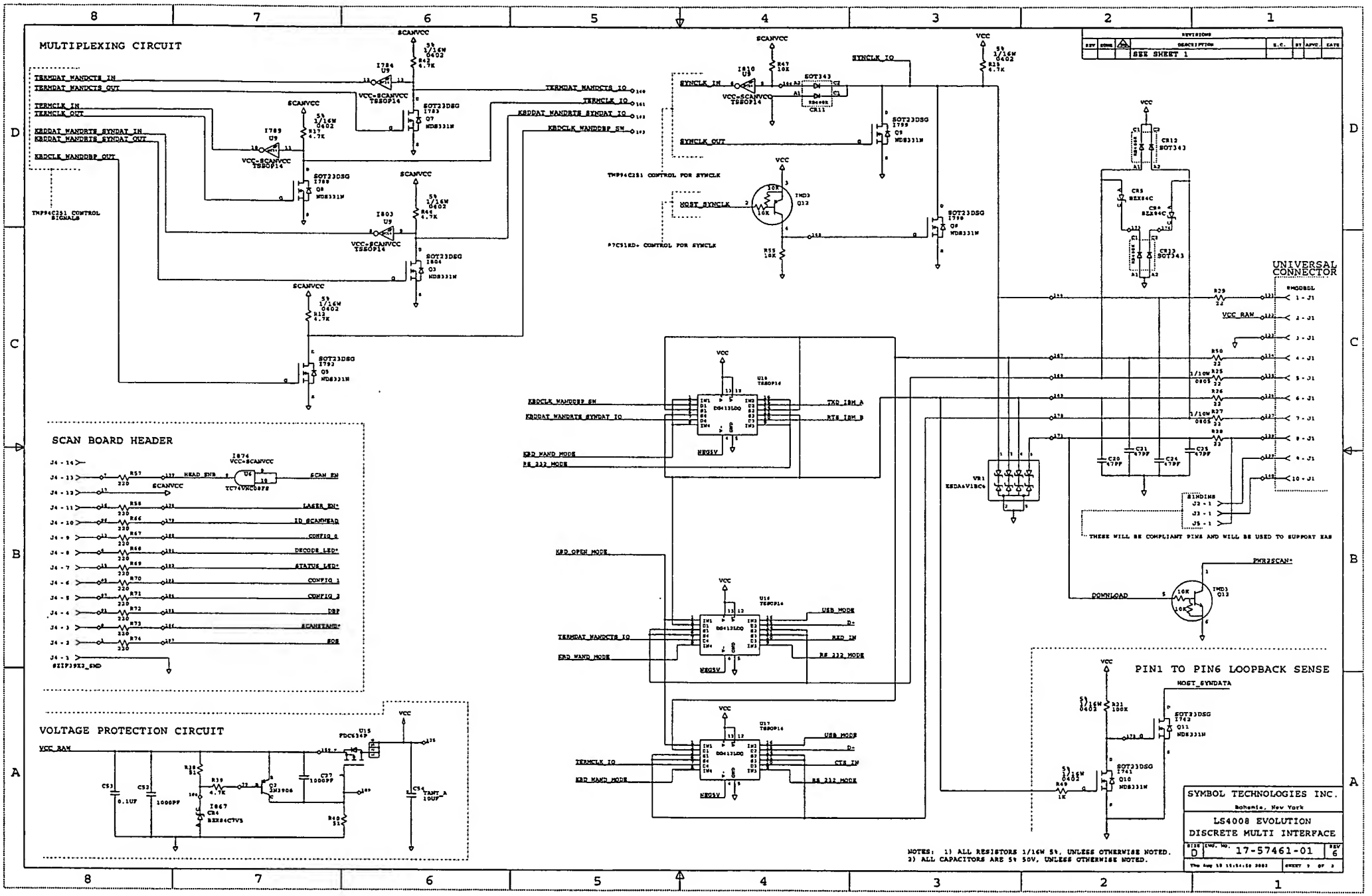
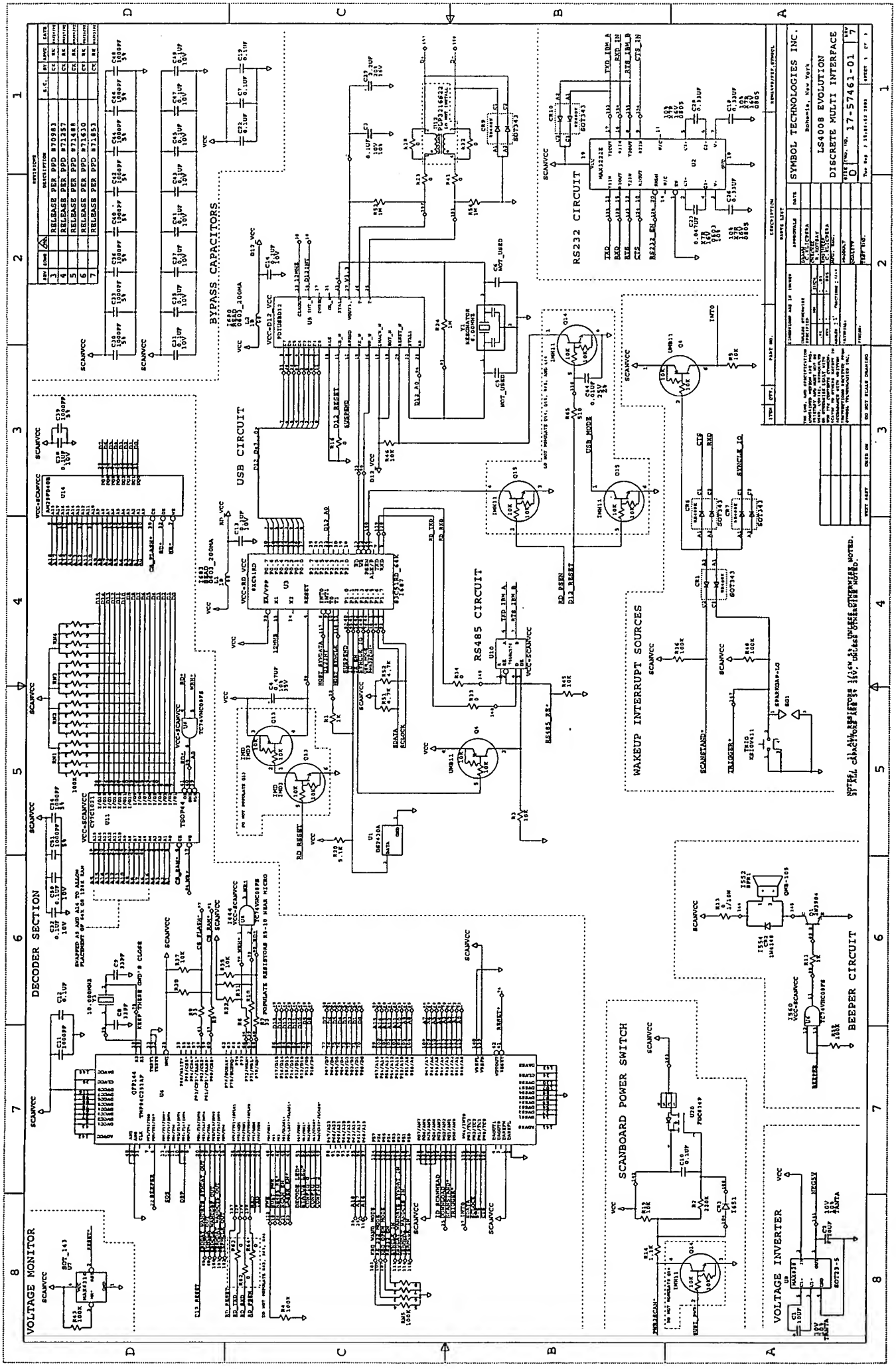

MULTIPLEXING CIRCUIT
SCAN BOARD HEADER
VOLTAGE PROTECTION CIRCUIT
UNIVERSAL CONNECTOR
PIN1 TO PIN6 LOOPBACK SENSE
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V, UNLESS OTHERWISE NOTED.

EXHIBIT NN


SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01
RELEASE PER PPD 870983
RELEASE PER PPD #71257
RELEASE PER PPD #71488
RELEASE PER PPD #71630
RELEASE PER PPD #71853
BYPASS CAPACITORS
USB CIRCUIT
RS232 CIRCUIT
RS485 CIRCUIT
WAKEUP INTERRUPT SOURCES
DECODER SECTION
SCANBOARD POWER SWITCH
BEEPER CIRCUIT
VOLTAGE INVERTER
VOLTAGE MONITOR

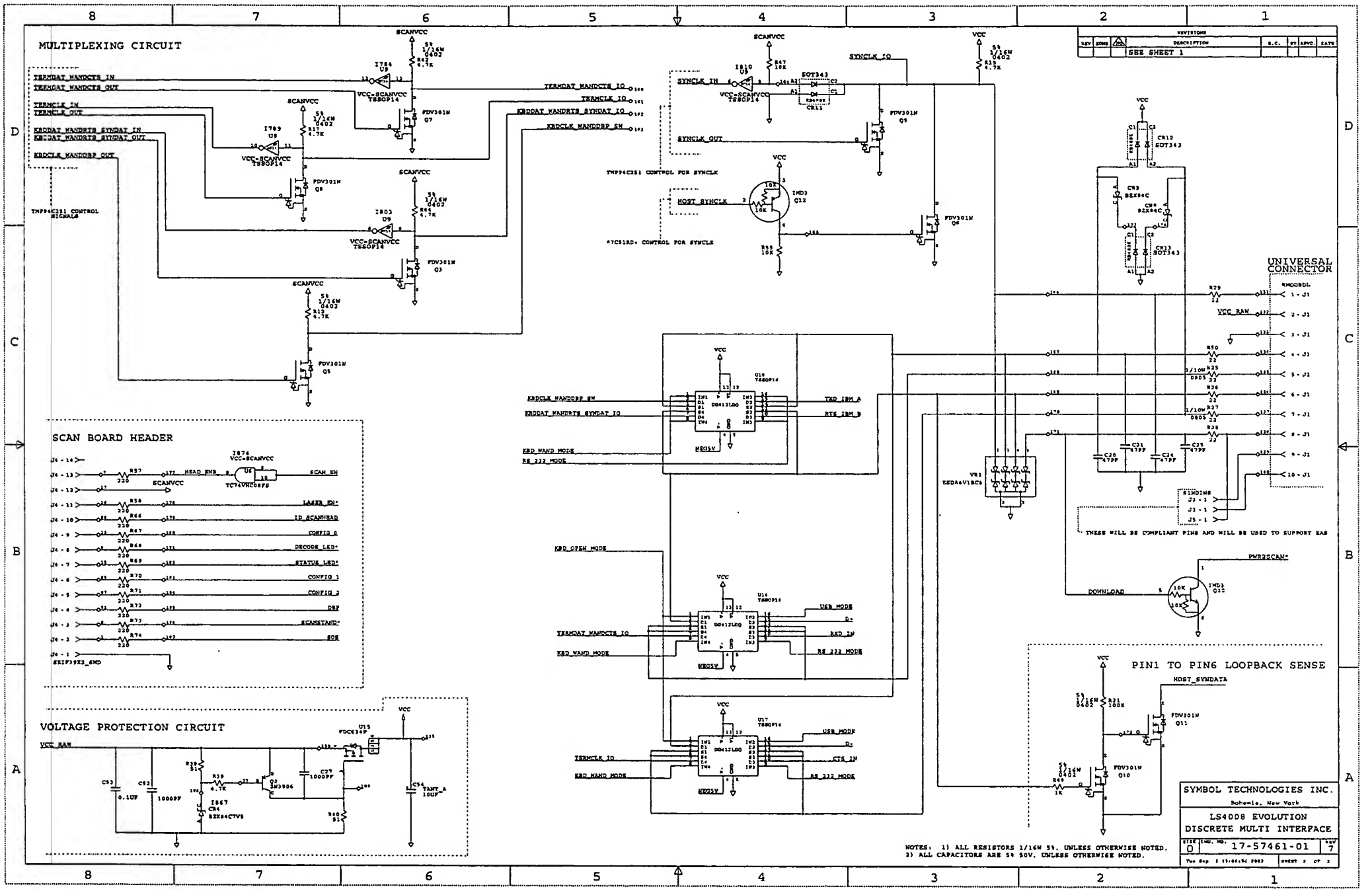
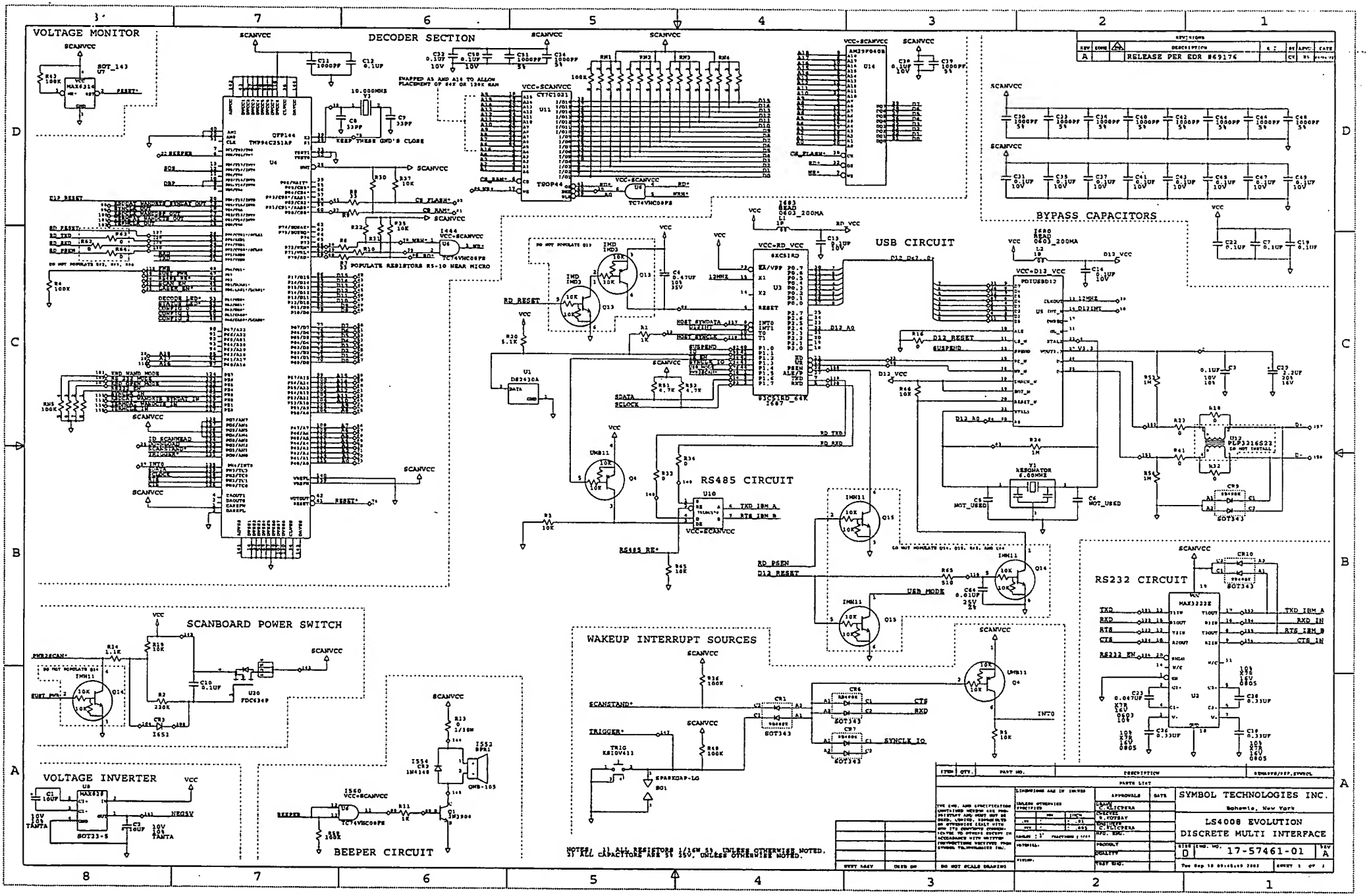

MULTIPLEXING CIRCUIT
SCANVCC
TERMDAT_WANDCTS_IN
TERMDAT_WANDCTS_OUT
TERMCLK_IN
TERMCLK_OUT
KBDDAT_WANDRTS_SYNDAT_IN
KBDDAT_WANDRTS_SYNDAT_OUT
KBDCLK_WANDDRP_OUT
TERMDAT_WANDCTS_IO
TERMCLK_IO
KBDDAT_WANDRTS_SYNDAT_IO
KBDCLK_WANDDRP_SW
SYNCLK_IO
SYNCLK_IN
SYNCLK_OUT
HOST_SYNCLK
TMP94C251 CONTROL FOR SYNCLK
TMP94C251 CONTROL SIGNALS
SCAN BOARD HEADER
VOLTAGE PROTECTION CIRCUIT
VCC_RAW
UNIVERSAL CONNECTOR
PIN1 TO PIN6 LOOPBACK SENSE
HOST_SYNDATA
KBD_OPEN_MODE
KBD_WAND_MODE
RS_232_MODE
TXD_IBM_A
RTS_IBM_B
RXD_IN
CTS_IN
DOWNLOAD
PWR2SCAN*
SCAN_EN
THESE WILL BE COMPLIANT PINS AND WILL BE USED TO SUPPORT EAS
NOTES: 1) ALL RESISTORS 1/16W 5%. UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V. UNLESS OTHERWISE NOTED.
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01

EXHIBIT OO


VOLTAGE MONITOR
DECODER SECTION
BYPASS CAPACITORS
USB CIRCUIT
RS485 CIRCUIT
RS232 CIRCUIT
SCANBOARD POWER SWITCH
WAKEUP INTERRUPT SOURCES
VOLTAGE INVERTER
BEEPER CIRCUIT
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01

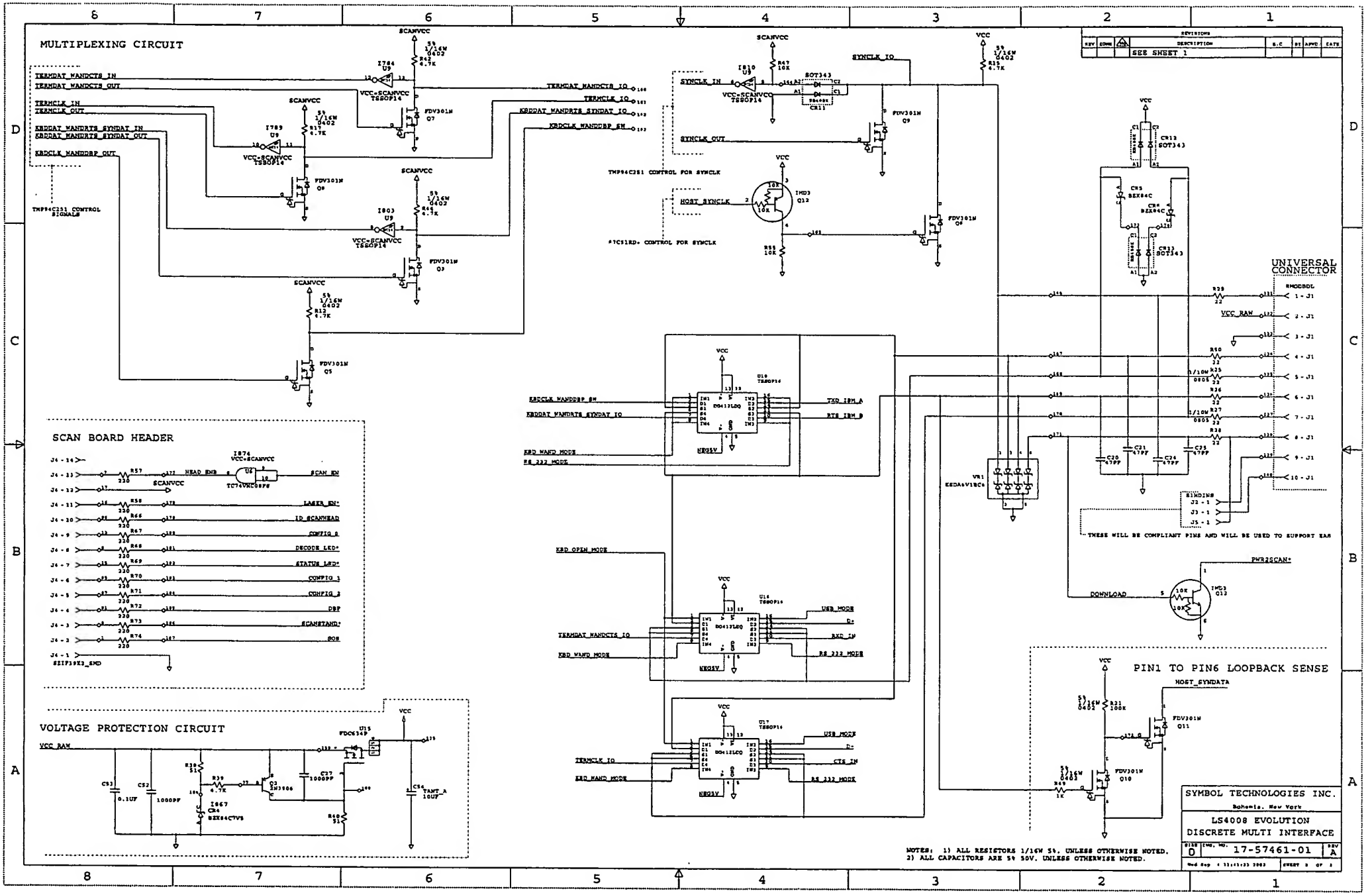

MULTIPLEXING CIRCUIT
SCAN BOARD HEADER
VOLTAGE PROTECTION CIRCUIT
UNIVERSAL CONNECTOR
PIN1 TO PIN6 LOOPBACK SENSE
SEE SHEET 1
SYMBOL TECHNOLOGIES INC.
Bohemia, New York
LS4008 EVOLUTION
DISCRETE MULTI INTERFACE
17-57461-01
NOTES: 1) ALL RESISTORS 1/16W 5%, UNLESS OTHERWISE NOTED.
2) ALL CAPACITORS ARE 5% 50V. UNLESS OTHERWISE NOTED.
THESE WILL BE COMPLIANT PINS AND WILL BE USED TO SUPPORT EAS

EXHIBIT PP

The attached diagram depicted is a suggestion to Olympus's design on LTIII and Spark II decoder electronics. The suggestions are the following:

a. Sharing of RXD and CTS RS-232 signals appear to be a better choice for multiplexing I/O pins. Since receivers of the MAX3222 are threshold at 0.8V. These receiver inputs can easily be clamped to VCC and GND using clamping diode in contrast to the active clamping circuit used in the current design. Hence, the KBDCLK and KDBDAT share with RXD and CTS in the diagram. In addition, this arrangement helps eliminate the additional analog switch used in the current design.
b. The TRMCLK and TRMDAT driving transistors used for Keyboard Wedge can also be used to send W_DBP and W_RTS while it is in Wand Emulation mode. The number of discrete driving/receiver pairs immediately reduced from six to four.
c. The only precaution needed is the SYN_DAT signal since it shares the same line as RTS. As what is appeared in the diagram, additional transistor can be used to isolate this signal from parasitic diode clamping inside the receiver inverter. The breakdown voltage of the driving MOSFET has to be able to sustain at least 10V (3.3 + 6) reverse voltage.

It is noted that the schematic in the diagram is provided for illustration purpose only. Some details are purposely omitted since they do not pertain to this discussion.

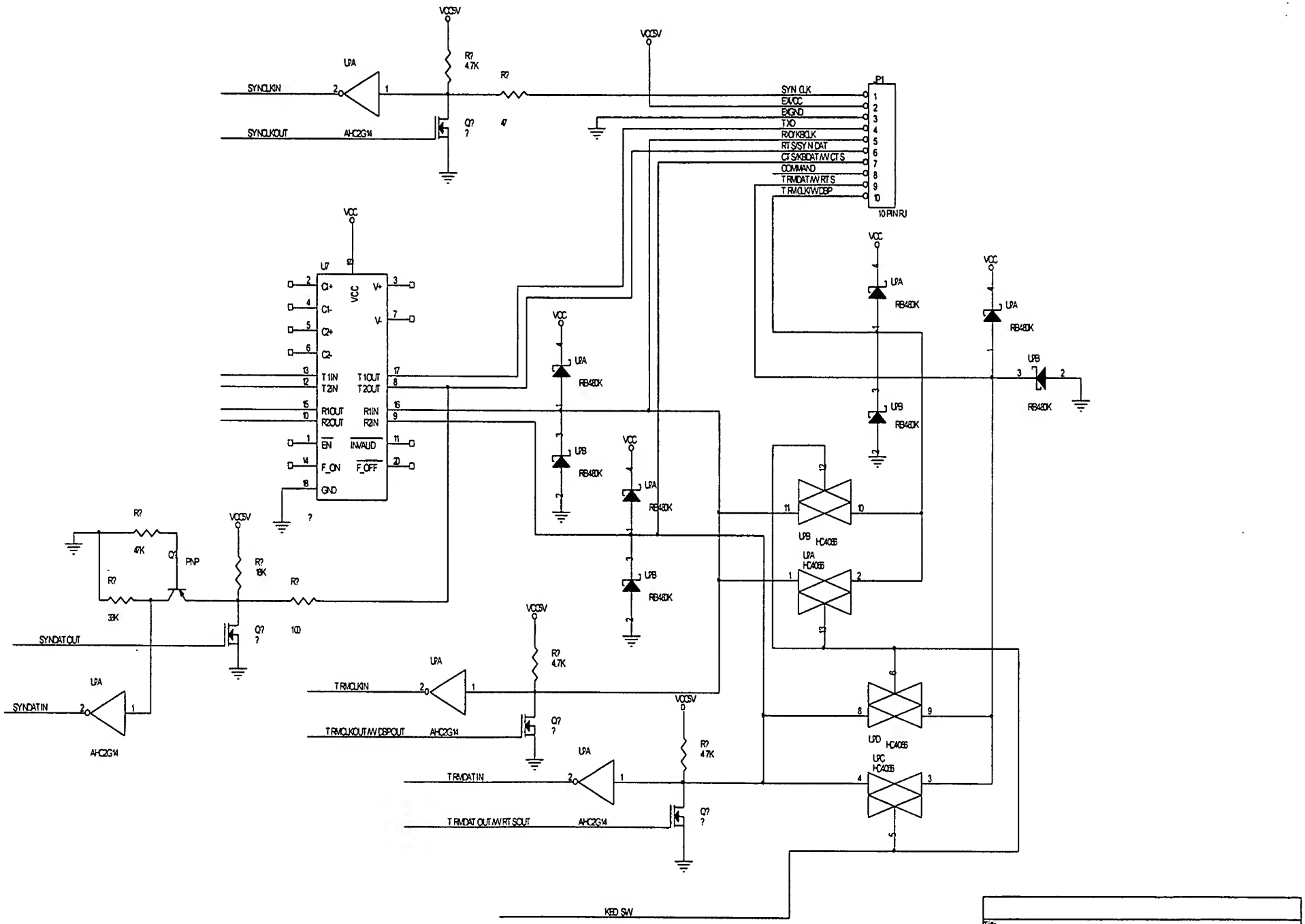

VCC5V
R?
4.7K
SYNCLKIN
SYNCLKOUT
U?A
AHC2G14
Q?
?
47
SYN CLK
EXVCC
EXGND
TXD
RXTKBCLK
RTS/SYN DAT
CTS/KBDAT/WCTS
COMMAND
TRMDAT/WRTS
TRMCLK/WDBP
P1
10 PIN RJ
VCC
U?
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
T1OUT
T2OUT
R1OUT
R2OUT
R1IN
R2IN
EN
INVAUD
F_ON
F_OFF
GND
U?A
RB480K
U?B
HC4066
47K
PNP
R?
18K
33K
100
SYNDATOUT
SYNDATIN
TRMCLKIN
TRMCLKOUT/WDBPOUT
TRMDATIN
TRMDATOUT/WRTSOUT
U?D
U?C
KEY SW
Title
{Title}
Size
B
Document Number
{Doc}
Rev
{Rev}
Date:
Thursday, September 14, 2000
Sheet
1
of
1

EXHIBIT QQ

Olympus's auto cable detection meeting 10/17/00

The Interfaces supported by the smart line (both LT III and Spark II) are:

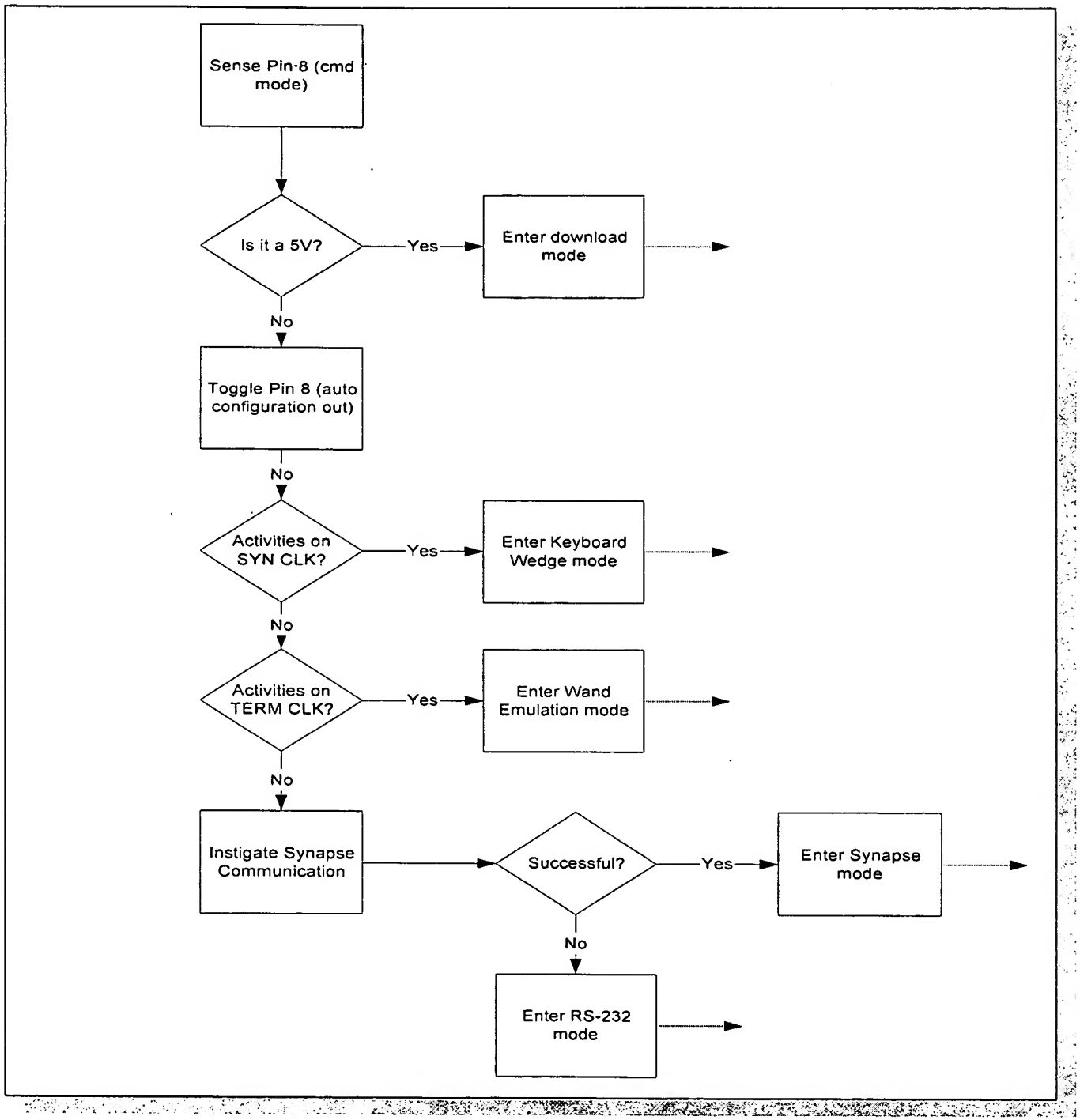
- RS-232
- Keyboard Wedge
- Wand Emulation
- Synapse
- USB (this interface only available on the USB model)

Currently, Olympus has proposed to add jumpers on both the Keyboard Wedge and Wand Emulation cables to auto detect attached cables on power up. Using the process-of-elimination the decoder micro can detect four out of five possible cables that may be attached to the unit. The following is Olympus suggested pin outs for the NG smart line design.

RS-232 Model						
		FLASH DL	SYN	RS232C	KBW	WAND
Pin	1	RXD	SYN_CLK		Auto config in	
Pin	2	VCC	VCC	VCC	VCC	VCC
Pin	3	GND	GND	GND	GND	GND
Pin	4			TXD	KBC_CLK	DBP
Pin	5			RXD		
Pin	6	TXD	SYN_DAT	RTS	KBD_DAT	RTS
Pin	7			CTS		
Pin	8	5V			Auto config out	Auto config out
Pin	9				TERM_DAT	CTS
Pin	10				TERM_CLK	Auto config in
		*	*	*		

Note: * cables already exist for Universal cable

Based on the above pin out, a possible cable detection flow is depicted as following:


Sense Pin-8 (cmd mode)
Is it a 5V?
Yes
Enter download mode
No
Toggle Pin 8 (auto configuration out)
No
Activities on SYN CLK?
Yes
Enter Keyboard Wedge mode
No
Activities on TERM CLK?
Yes
Enter Wand Emulation mode
No
Instigate Synapse Communication
Successful?
Yes
Enter Synapse mode
No
Enter RS-232 mode

Some issues need to be discussed prior to giving Olympus a "go ahead" on realizing their proposal:

- Is the proposed cable detection scheme reliable enough?
- If not, is there any way to improve the likelihood of reliable detection? What are the concerns regarding to this detection scheme?
- Marketing would like to retain the feature of being able to identify attached cable. Is there another feasible implementation available?
- How will this cable detection scheme handle new cable(s) to the universal cable family?

EXHIBIT RR

Minutes from Olympus automatic cable detection meeting on Oct. 17, 2000

Attendee: Mike Catalano
Rob Lieb
Foong Chin
Rizwan Alladin
Mike Rizzi
Rich Wienecke
Tony Chang

The purpose of this meeting is to review the cable detection scheme proposed by Olympus in the NG Smart line design. Moreover, it has to take into consideration the effect of future products as result of this outcome. More importantly, it needs to ascertain these added jumpers are not going to hinder the development of the future products. As a result of this meeting, it is concluded that Olympus cable detection scheme is not robust enough. The reasons are as following:

1. Mike Rizzi stated that driving the TERM_CLK signal during PC power up could cause PC to produce long hasty beeps, which is probably not desirable for Keyboard Wedge users. Mike had experience working with Phaser 302.

2. The wiggling of SYNC_CLK signal by the Synapse lump can easily be misinterpreted for cable detection signal issued from AUTO CONFIG OUT pin. The risk of wrong detection would be high unless the detection initiates only after failing the Synapse connection. By then, it is 100% sure that is no other interface would drive this signal.

3. The occurrence of signals on the standard PC keyboard could be spontaneous (e.g. keyboard test during boot-up, or as if someone presses key) so that the state of TERM_CLK is unpredictable. Hence, using TERM_CLK to pass signal for cable identification is undesirable.

4. This detection scheme proposed by Olympus does not allow for future cable expansions. There is no signal pin available, which are similar to SYN_CLK or TERM_CLK, to be reserved for future cables. All the rest signal pins are currently shared among multiple interfaces. As we know, there are at lease two cables (USB and IBM468x) that are not accounted for by the design of RS-232 model. These two cables are part of universal cable family and will soon be integrated with the other cables soon after the multi-interface ASIC becomes available.

5. Suggestion of using KEY_CLK and KEY_DAT signal on power up was also explored in this meeting. The group discussed the possibility of momentarily disconnecting the keyboard from terminal (PC) to allow cable detection being done on these signals. The downside to this approach was the side effect of sending erroneous setup message to the keyboard. This would result in wrong keyboard settings after power up.

<u>Other schemes that has been explored in the meeting are</u>:

Rob and Rich suggested the detection process by starting with intelligent interface host first, such as USB, Synapse. Then, try to re-use pins that are vacant after this process-of-elimination to detect the reset of cables. The group concluded the drawback to this approach would be its fragility rigidity and degree of uncertainty from some interface function like USB, in its implementation as well as sluggishness due to its aggregate delays from multiple interface attempts.

Mike Catalano proposed to embed resistor in each individual cable as a way to identify them. The decoder or interface micro will then make use of its unused resources, such as timer counter, to discern resistor value so as to identify cables. This detection scheme will only detect the resistor value through the download signal pin. Therefore, it would not put any burden to the already congested signal/pin

arrangement. But, the catch to this approach would be that it forces to retrofit all of the existing universal cables.

The group didn't conclude whether added jumper in each cable would obstruct the development of new product, which will be using these cables. Mike Rizzi raised the concern about future ramification on the EAS cable implementation.

Please don't hesitate to contact me if you find any discrepancy in this minutes or if I have miss out anything that transpired in that meeting. Thank you again for sparing your time to attend this meeting.

EXHIBIT SS

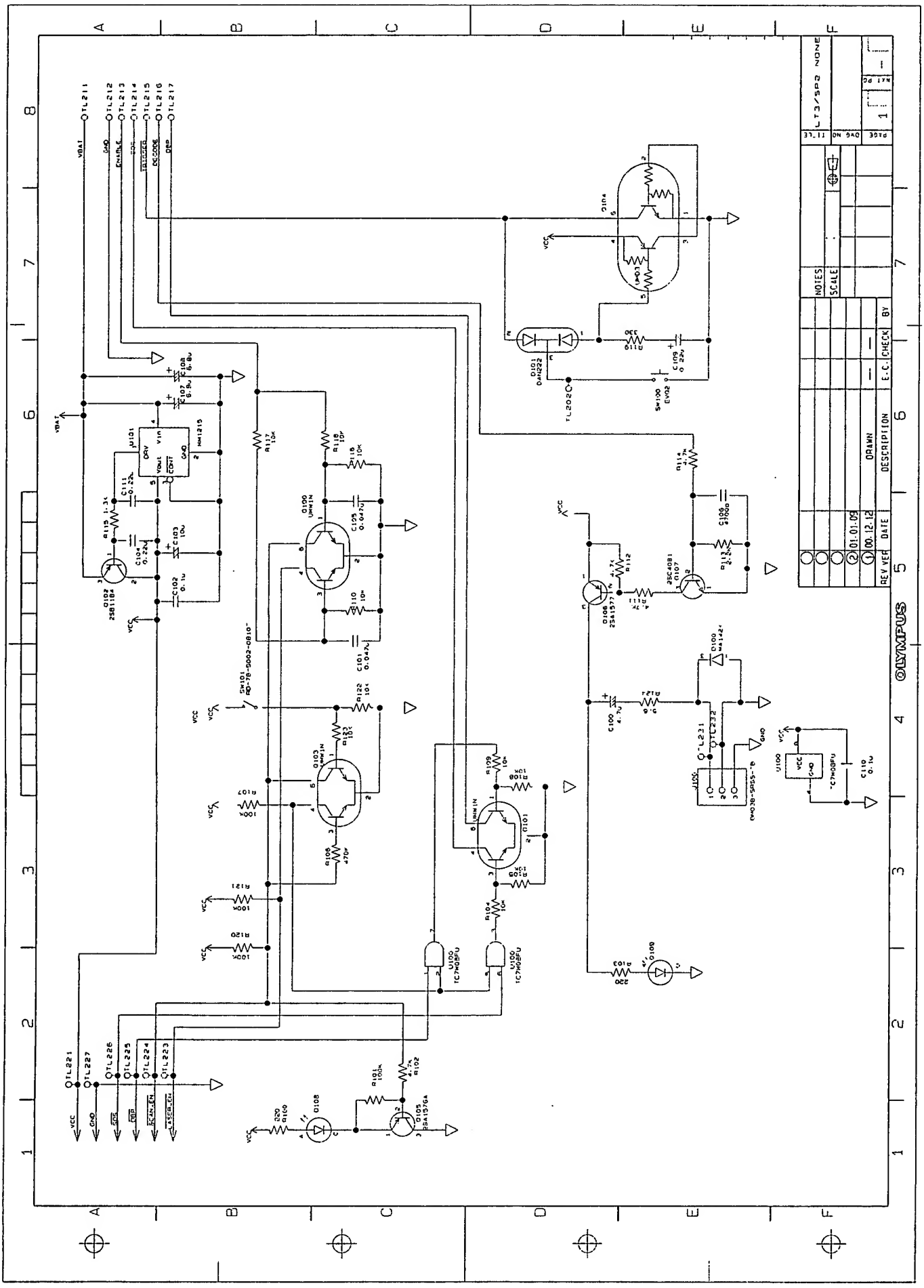

OLYMPUS
DRAWN
DESCRIPTION
DATE
E.C.
CHECK
BY
NOTES
SCALE
2001.01.09
1000.12.12
TL211
TL212
TL213
TL214
TL215
TL216
TL217
TL221
TL227
TL226
TL225
TL224
TL223
TL202
SW100
SW101
U100
U101
U102
U103
U104
U105
U106
U107
U108
U109
U110
U111
U112
U113
U114
U115
U116
U117
U118
U119
U120
U121
U122
U123
U124
U125
U126
U127
U128
U129
U130
U131
U132
U133
U134
U135
U136
U137
U138
U139

EXHIBIT TT

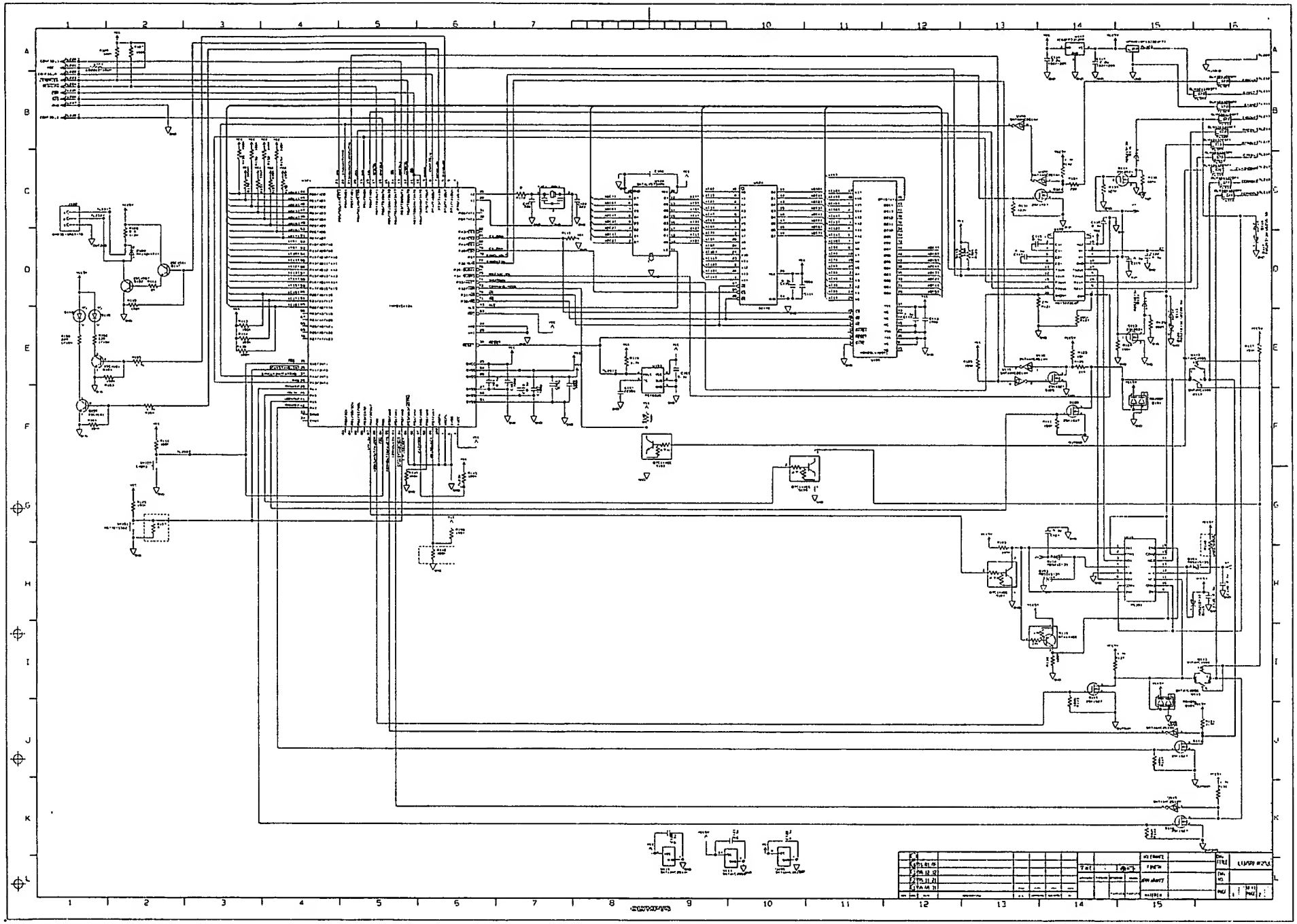
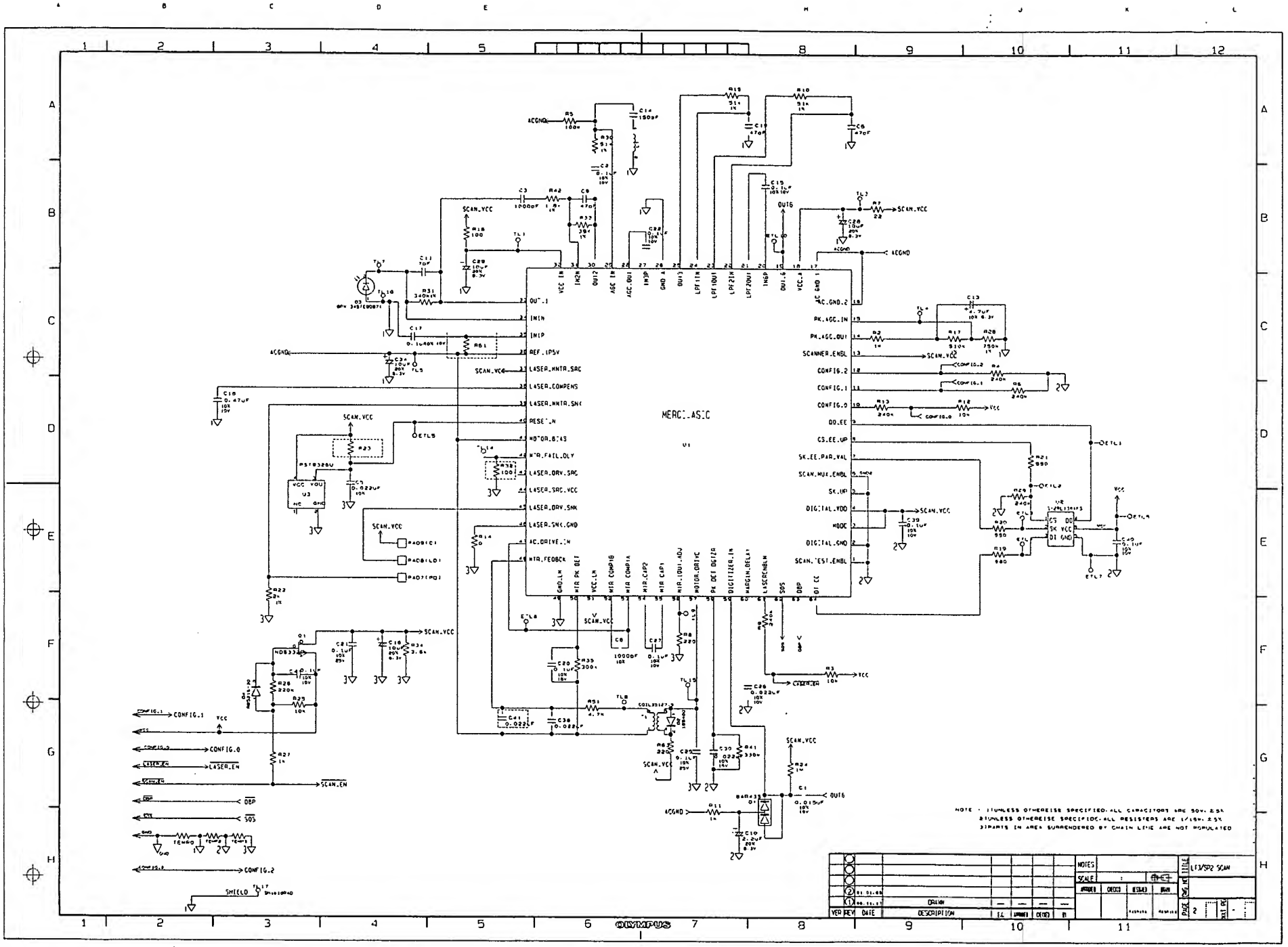


EXHIBIT UU


MERC_ASIC
U1
SCAN_VCC
ACGND
CONFIG.1
CONFIG.0
CONFIG.2
LASER_EN
SCAN_EN
SMIELD
OLYMPUS
NOTES
SCALE
LF3/SP2 SCAN